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Epitaxy of gallium nitride films on silicon substrates

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ABSTRACT OF THE MASTER'S THESIS

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Metal organic vapour phase epitaxy (MOVPE) of c-plane gallium nitride (GaN) on 6-inch (111) silicon substrates is studied in this thesis. GaN layers were grown by an Aixtron 6" CSS MOVPE employing an aluminium nitride nucleation layer and a step graded aluminium gallium nitride buffer layer. The epitaxial layer thicknesses were mapped over the whole wafer with a spectrophotometer. The total film thickness was approximately 2.05 μm. The thickness uniformity was good and the standard deviation was 1.1% (10 mm edge exclusion). The wafer geometry was measured using capacitive profiling. The wafer bow was 80.1 μm after growth. The bow was non-spherical probably due to thickness non-uniformity. Reciprocal space maps around (002) and (105) reflections were measured with x-ray diffraction. The GaN layers were under tensile strain at room temperature. The full width at half maximum of the (002) and (105) ω-scans were 800 and 770 arcsec, respectively. To further improve the structure a thicker buffer layer possibly with higher aluminium content should be used to reduce wafer bow. Also dislocation reduction techniques such as SiN_x interlayers should be considered to increase crystal quality. In addition, aluminium predose instead of nitridation could be employed.

Keywords: gallium nitride, metal-organic vapour phase epitaxy

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Tässä diplomityössä tutkitaan c-kidetason galliumnitridin (GaN) valmistusta metallo-organisella kaasufaasiepitaksialla (MOVPE) 6:n tuuman (111)-piialustakiteille. GaN-kerrokset valmistettiin Aixtron 6" CCS MOVPE -laitteella käyttäen alumiininitridiydintymiskerrosta ja porrastettua alumiinigalliumnitridipuskurikerrosta. Valmistettujen kerroksien paksuus mitattiin koko kiekon alueelta valkoisen valon heijastusmittauksella. Valmistettujen kerrosten yhteinen paksuus oli noin 2,05 μm ja kerrospaksuuden keskihajonta oli 1,1% (tuloksesta poistettu 10 mm kiekon ulkoreunalta lukien). Kiekon geometria mitattiin kapasitiivisella profiloinnilla ja havaittiin, että kiekon kaarevuus oli 80,1 μm. Kaarevuus ei ollut täysin ympyräsymmetrinen johtuen todennäköisesti valmistetun kerroksen paksuusvaihtelusta. Röntgendiffraktiolla mitattiin (002)- ja (105)-heijastuksista käänteishilakartat, joiden perusteella GaN-kerrokset olivat vetojännitystilassa huoneenlämmössä. Puoliarvoleveydet (002)- ja (105)-heijastuksille olivat 800 ja 770 kaarisekuntia. Rakennetta voitaisiin parantaa käyttämällä paksumpaa puskurikerrosta tai lisäämällä alumiinin määrää kerroksissa. Kidevirheiden määrää pitäisi pienentää esimerkiksi käyttämällä piinitridivälikerroksia. Prosessi voitaisiin myös aloittaa atomaarisella alumiinipäällystyksellä pinnan nitrauksen sijaan.

Avainsanat: Galliumnitridi, metallo-organinen kaasufaasiepitaksia

Preface

This Master's thesis was conducted at the Aalto University, School of Electrical Engineering, Department of Micro- and Nanosciences, Optoelectronics research group. I would like to thank Professor Markku Sopanen for the opportunity to write my thesis on this exciting topic. I wish to thank my advisor D.Sc Sami Suihkonen for interesting discussions on all things scientific and general, expertise, help and guidance during this work. I wish to thank D.Sc Atte Haapalinna and Okmetic Oyj for providing high quality silicon substrates vital for this study and for organising the wafer geometry measurements.

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Contents

Abstract ii

Abstract (in Finnish) iii

Preface iv

Contents v

Abbreviations vii

1 Introduction 1

2 Crystalline semiconductors 3
- 2.1 Crystal lattice . . . 3
- 2.2 Semiconductors . . . 5
- 2.3 Compound semiconductors . . . 7
- 2.4 Gallium nitride . . . 8

3 MOVPE 11
- 3.1 Operation . . . 11
- 3.2 Growth mode . . . 13
- 3.3 Growth regime . . . 14
- 3.4 Growth of GaN . . . 15
- 3.5 Substrates for GaN epitaxy . . . 16

4 Aixtron 1x6" CCS MOVPE 19
- 4.1 System . . . 19
- 4.2 In situ monitoring . . . 20

5 Characterization methods 25
- 5.1 Spectrophotometer . . . 25
- 5.2 X-ray diffraction . . . 26
- 5.3 Wafer geometry measurement . . . 29

6 Gallium nitride on silicon 30
- 6.1 Substrate orientation . . . 30
- 6.2 Buffer layers . . . 31
- 6.3 Wafer bending . . . 31
- 6.4 Crystal quality . . . 33

7 Results 34
- 7.1 Optimizing growth . . . 34
- 7.2 Growth process . . . 36
- 7.3 Layer thickness . . . 38
- 7.4 Wafer geometry . . . 40

7.5 X-ray diffraction 41

8 Conclusion **44**

References **45**

Abbreviations

2D	two-dimensional
3D	three-dimensional
Al	aluminium
AlGaN	aluminium gallium arsenide
AlN	aluminium nitride
CCD	charge-coupled device
CCS	close coupled showerhead
CMOS	complementary metal oxide semiconductor
ELOG	epitaxial layer overgrowth
FET	field effect transistor
FM	Frank-van der Merwe
FWHM	full width at half maximum
Ga	gallium
GaAs	gallium arsenide
GaAsP	gallium arsenide phosphide
GaN	gallium nitride
HEMT	high electron mobility transistor
HRXRD	high resolution x-ray diffraction
HVPE	hydride vapour phase epitaxy
InN	indium nitride
InP	indium phosphide
LD	laser diode
LED	light emitting diode
MBE	molecular beam epitaxy
MEMS	micro electro mechanical system
Mg	magnesium
MOVPE	metal organic vapour phase epitaxy
N	nitrogen
RSM	reciprocal space map
Si	silicon
SiC	silicon carbide
SK	Stranski-Krastanov
TEGa	triethylgallium
TMAl	Trimethylaluminum
TMGa	Trimethylgallium
TMIn	Trimethylaluminum
UV	ultraviolet
VW	Volmer-Weber
XRD	x-ray diffraction

1 Introduction

Gallium nitride (GaN) is a compound semiconductor that belongs to the nitride subset of III-V compound semiconductors. GaN has become the second most important semiconductor after silicon (Si) [1]. The electrical and physical properties, such as the direct and wide bandgap in addition to good thermal and chemical stability, make GaN a highly interesting material [2].

The direct bandgap allows efficient optoelectronic applications. GaN based blue light emitting diodes (LED) have received attention [3]. Blue LEDs can be, in turn, used to create white LEDs. This is done by converting some of the emission to longer wavelengths, usually by using different phosphorous coatings [3]. The result is a LED whose emission resembles white light. An efficient while light source can reduce the energy consumption of lighting tremendously. In fact, the GaN based white LEDs have seen increasing deployment for this application [3]. The GaN LED offers higher energy efficiency and longer lifetime than an incandescent bulb. The importance is highlighted by the 2014 nobel price in physics which was awarded for developing the blue GaN LED [4]. In addition, GaN based blue laser diodes (LD) are commonly used in Blu-Ray optical disk data storage devices.

The wide band gap of GaN also results in a high breakdown field [5]. This combined with good thermal stability, heat conductivity and high electron mobility make GaN an excellent candidate for high performance electrical applications. Indeed, GaN based devices are seeing increasing deployment for radio base-station and radar applications [6]. In these applications, high power densities and high frequencies are required. GaN based high electron mobility transistor (HEMT) is suited for these challenges. A GaN HEMT exhibits high cut-off frequency and low on-resistance [6]. Previously gallium arsenide (GaAs) based HEMTs were used. While GaAs has higher electron mobility, GaN has considerably higher breakdown field than GaAs. This means that a GaN amplifier can reach the same performance with less transistor stages.

In addition to radio applications, GaN is predicted to take over some part of power electronics such as frequency converters [7]. In these applications, the high sustainable power density and low on-resistance allows increased performance and efficiency [7]. Currently, most power electronic devices are based on either Si or silicon carbide (SiC). GaN offers higher performance compared to Si and lower device cost than SiC. However, SiC has higher breakdown field. Therefore, it seems that GaN is most suited for the voltage range between those of Si and SiC [5].

There has been an interest of manufacturing III-nitride (III-N) compounds since the semiconducting properties of III-V compounds were predicted in 1952 [8]. However, growth of GaN has proven difficult. Indeed, the first GaN LED was not demonstrated until 1971 [9]. In stark contrast, a red GaAsP LD was realized in 1962 [10]. The growth of high quality GaN is limited by the lack of suitable substrates. Foreign substrates typically have either a vastly different lattice constant or a different atomic arrangement compared to GaN. Moreover, common melt based growth processes cannot be used to grow bulk GaN substrates. Instead, GaN devices are almost exclusively grown on Si, sapphire or SiC [1, 3]. The difficulty of growing

bulk GaN is due to the fact that GaN sublimates at atmospheric pressure instead of melting. It should be noted that native GaN substrates have been grown at extreme temperature and pressure conditions [11]. However, typically the size and quality of these substrates is not sufficient for commercial devices [11].

Metal-organic vapour phase epitaxy (MOVPE) is the most used method for III-N device growth [5]. MOVPE offers reasonably high growth rates with good material quality and multiple material compositions. Other methods such as molecular beam epitaxy (MBE) or hydride vapour phase epitaxy (HVPE) also exist. MBE offers lower impurity incorporation although at lower growth rates than MOVPE. On the other hand, HVPE has a higher growth rate than MOVPE but the achievable material compositions and crystal quality limit the usefulness of HVPE. At present, most commercial devices are processed with MOVPE, MBE is employed for materials research and HVPE is used to manufacture bulk GaN substrates [5].

Widespread use of GaN requires low device cost [1]. One way to decrease the cost is to use cheaper substrates. In addition, the use of larger substrates decreases the processing cost. The processing time and resources are almost independent of the wafer size but there are more chips per wafer on a larger wafer. Silicon substrates suitable for GaN growth are available at 8-inch size. Silicon substrates are considerably cheap, the price is about 1/10 of that of a sapphire substrate and about 1/100 of that of a SiC substrate [12]. In addition, it is suggested that some obsolete silicon device processing facilities could be re-purposed for GaN on Si device processing. However, growth of GaN on Si is challenging and the crystal quality is lower than for growth on sapphire or SiC. Therefore, it seems that GaN on Si is suitable for lower cost applications which still can benefit from the properties of GaN. These include lower voltage power electronics and general lighting where the acquisition cost is important [13].

Growth of GaN on Si is challenging because of the vastly different material properties. Indeed, the first GaN on Si LED was demonstrated as late as 1998 [14]. There is a considerable lattice mismatch (18%) and large thermal expansion coefficient mismatch (46%) between GaN and Si [2]. Moreover, GaN cannot be directly grown on silicon because gallium reacts aggressively with silicon at elevated temperatures [5]. Despite these challenges, device quality GaN can be realized on Si using appropriate intermediate layers. The lattice and thermal expansion mismatch can lead to high stresses and bowed wafers. Therefore, wafer bow and stress tailoring are required during growth [13]. In addition, the high initial dislocation density caused by the lattice mismatch needs to be reduced during growth.

The aim of this thesis is to study the MOVPE growth of GaN films on silicon. Firstly, the properties and MOVPE growth of GaN are introduced. A modern MOVPE apparatus for GaN on Si growth by Aixtron is presented. The apparatus is intended for growth on 6-inch silicon substrates. Then, the peculiarities of GaN on Si are discussed. GaN on Si growth process employing an AlGaN buffer layer scheme is discussed. Finally, the characterization of the grown structure is presented. White light reflection is used to assess layer thickness and the wafer profile is measured for the amount of bow after growth. The material quality is analysed with x-ray diffraction measurements.

2 Crystalline semiconductors

The aim of this chapter is to present the properties of crystalline solids and physics of semiconductors in order to understand the properties of gallium nitride. First, the concept of crystal lattice, lattice directions and planes are described. Then, general properties of semiconductors are presented followed by compound semiconductors. Finally, gallium nitride is considered from these perspectives.

2.1 Crystal lattice

Crystalline solids are materials that have ordered periodical structure in three dimensions unlike amorphous materials which lack long period ordering. Some materials can exist in different crystal or amorphous arrangements. However, certain materials are thermodynamically stable only in a form of a crystal. For example, GaN melt cannot be created at atmospheric pressure.

Single crystalline materials maintain the ordering in a certain piece of that material. On the other hand, polycrystalline materials have several regions that are periodically arranged. These regions, grains, are then misaligned with respect to one another. Therefore, the periodicity is not satisfied at the grain boundaries.

The atoms within a crystal are ordered so that the various inter-atomic distances and orientations are constant throughout the material. The particular set of periodic arrangements of atoms is called a lattice. There are 14 possible different lattices [15].

Lattices are defined by unit cells. The unit cell is the smallest periodic arrangement of atoms in a certain lattice. The entire lattice can be then constructed by placing unit cells next to each other. The unit cell is span by lattice vectors. Three vectors are required to span a three dimensional space. Lattice vector translation from a lattice site leads to a similar lattice site. In other words, the lattice can be constructed using lattice vectors in addition to using unit cells. The magnitudes of lattice vectors are called lattice constants.

Direction of a line in a lattice is typically described using the unit vectors. Figure 1 presents some directions in a lattice. A line passing through the origin and a point (u,v,w) can be described as having the direction of (uvw). Any direction can be then described this way by first drawing a parallel line through the origin. Note that the indices u v w are not necessarily integers. However, the indices can be converted to the smallest possible set of integers. Therefore $[\frac{1}{2}\frac{1}{2}1]$, [112] and [224] represent the same direction. However, [112] is the preferred form. Negative indices are written with a bar over the number, for example $[\bar{1}12]$.

Miller indices are used to distinguish crystallographic planes. Figure 2 presents some Miller indices of planes in a cubic crystal. Consider a plane in a lattice which dissects a unit cell with lattice vectors **a**, **b** and **c**. Now, the plane intersects the axes of the unit cell. The distance of the intersection points x, y and z are measured along the lattice vectors from the origin. Next, the respective lattice vector length is divided with the interception point distance from the origin. Thus, (hkl) $= (\frac{|\mathbf{a}|}{x}, \frac{|\mathbf{b}|}{y}, \frac{|\mathbf{c}|}{z})$. This is convenient as the lattice vectors can have different lengths. In addition, a plane that is perpendicular to a certain crystallographic axis has the Miller index

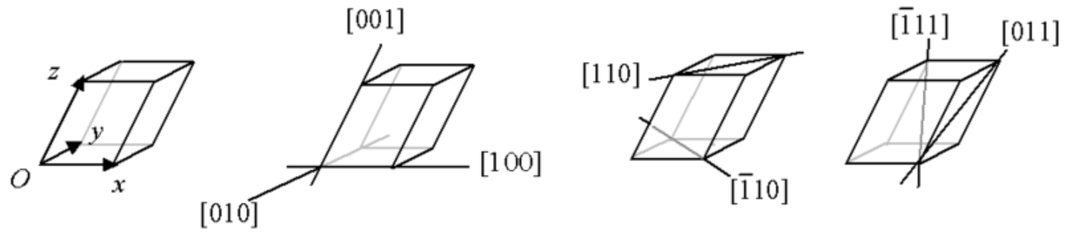


Figure 1: Various lattice directions [16].

of zero. In short, the Miller indices are defined as the reciprocals of the fractional intercepts that the plane has with the lattice vectors. Similar to lattice directions, a negative Miller index is denoted with a bar over the number.

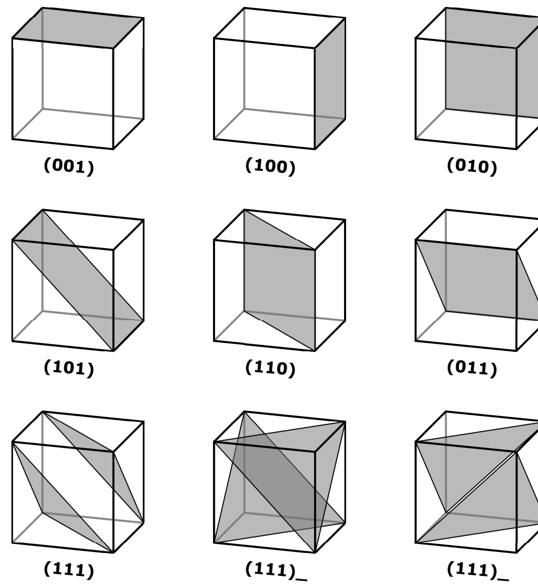


Figure 2: Miller indices in a cubic system [17].

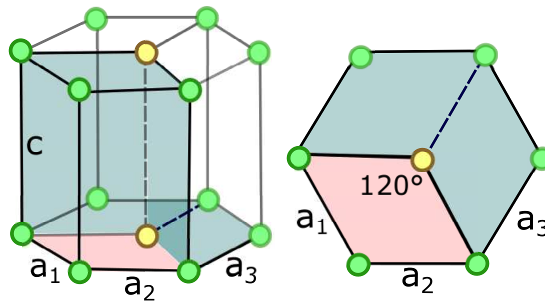


Figure 3: Hexagonal lattice with one unit cell highlighted. Adapted from reference 18.

Hexagonal crystal system can be indexed similarly, although a four index notation (hkil) is also commonly used. As any crystal, the hexagonal system can be

defined using three lattice vectors hkl. The fourth index i highlights the crystal symmetry. Figure 3 presents the hexagonal lattice. One rhombic unit cell of the hexagon is highlighted. Three unit cells are required to complete the hexagonal atomic arrangement.

In the case of the four index notation, three vectors $\mathbf{a_1}, \mathbf{a_2}$ and $\mathbf{a_3}$ define a basal plane. The angle between these vectors is 120° and $|\mathbf{a_i}| = a$. This angle results in a six-fold symmetry of the crystal. It also follows that -i = h + k. The fourth lattice vector **c** is perpendicular to the basal plane and it defines the separation of two basal planes.

2.2 Semiconductors

Semiconductors are materials whose conduction properties can be altered. In a crystalline semiconductor electrons cannot have arbitrary combinations of momentum and energy. Instead, the electrons typically reside in two energy regions that are separated. The electrons can transfer between these regions if the electron energy is altered sufficiently.

The energy regions are typically explained using the energy band model. The energy band model can be derived from quantum mechanical considerations. The electronic binding force between the atom core and the electrons can be simplified to a potential well. Now, when a vast amount to atoms are brought to close proximity, the potential wells start to overlap. The electrons closest to the core are still tightly bound. However, the electrons that are close to the well edges are no longer effected by only one core. A periodic potential is formed whose properties are defined by the inter-atomic distance and electric attraction. This periodic potential allows some electrons within a specific energy range to tunnel through the potential barriers. Thus, some electrons can move in the material. However, the electrons cannot have the same wavenumbers as stated by the Pauli exclusion principle. Therefore, a continuous spectrum of electron energies is formed around the suitable energy value for tunneling, and it is called an energy band.

The concept of Fermi level is closely related to electronic band structure. The Fermi level is defined as the highest energy that the electrons occupy at 0K or the energy where the occupation probability is 50%. In the case of intrinsic or moderately impure semiconductors, the Fermi level is located between two energy bands. The band above the Fermi level is called the conduction band. Conversely, the band below the Fermi level is called the valence band. The energy region between the bands without electrons is called the band gap. It should be noted that for high impurity concentrations, the Fermi level can coincide with a band.

The energy band model can be used to explain electrical and optical properties of a material. An empty or a full band cannot conduct electricity. Either electrons or local deficit of electrons can contribute to an electrical current. The lack of one electron is typically modelled as a quasi particle with a positive charge called a hole. Together electrons and holes are referred to as charge carriers.

In metals, the Fermi level resides within a band. Therefore, the highest band is partially filled, which explains the good conductivity. On the other hand, insulators

have a large energy separation, band gap, between the bands. In addition, only the valence band is filled with electrons. Thus, the electrical conductivity of insulators is low. Semiconductors are somewhere between these two extremes. The band gap of semiconductors is smaller than the band gap of insulators. At low temperatures, semiconductors work as insulators. However, at room temperature, thermal energy is usually sufficient to excite electrons to the conduction band from the valence band. As a result, semiconductors show some conducting properties.

The division of materials to semiconductors and insulators is somewhat arbitrary. Semiconductors are characterized by their usefulness in electrical components. For these applications it is required that the density of electrons between the bands can be altered.

The electrical properties of semiconductors can be altered by introducing minute amount other suitable materials into the semiconductor lattice. This process is called doping. If atoms with more valence electrons than the host material are introduced, the Fermi level is effectively raised. Thus, the valence band becomes filled and the excess electrons are raised to the conduction band. This type of semiconductor is called n-type where the majority charge carrier is an electron. The conduction in an n-type material arises from the partially filled conduction band with excess electrons. On the other hand, if atoms with less valence electrons are introduced, p-type material is created. A p-type material has a lower Fermi level and the majority charge carrier is a hole. In the case of a p-type material, the conduction is caused by the holes in the partially filled valence band.

Optical properties of semiconductors can be explained using the magnitude and alignment of the band gap. Electrons can be excited from the valence band to the conduction band if sufficient energy is provided. Therefore, only photons with equal or greater energy than material band gap have significant absorption. Similarly, a semiconductor most likely emits photons with with an energy close to the band gap energy.

The band alignment significantly affects the photon absorption probability. In a direct band gap material, electrons can be excited directly from the valence band to the unoccupied states of the conduction band. However, in a indirect band gap material, the valence band maximum and the conduction band minimum are not located at the same electron momentum. Therefore, the electron momentum must also be changed in the absorption process. Photon momentum is small compared to the electron momentum. The impulse is provided by a phonon, the quantum of lattice vibration. This simultaneous interaction of an electron with a photon and a phonon is considerably less probable than excitation in the case of the direct band gap. Thus, the absorption and emission in indirect band gap semiconductors is weak compared to those in direct band gap materials. In optoelectronic applications, direct band gap materials are preferred. However, it can be beneficial to employ indirect band gap materials in segments where either absorption or emission is unwanted.

2.3 Compound semiconductors

Compound semiconductors are material systems that consist of two or more types of atoms. The most commonly used material systems in optoelectronic applications are the III-V semiconductors. The III-V semiconductors consist of group III and group V elements. These elements do not exhibit semiconducting properties by themselves. In addition, typically the physical properties of these elements differ significantly. For example, aluminium is a commonly used metal and nitrogen is a gas. Still, these two elements can form aluminium nitride under suitable conditions. Only when brought together into a thermodynamically stable lattice the semiconducting properties appear.

The history of compound semiconductors starts in the early 20th century. Although the III-nitride based devices have a shorter history than the III-arsenide or III-phosphide applications, the nitride compounds were discovered first. AlN, InN and GaN were first reported in 1907, 1910 and 1932 [19], respectively. The semiconducting properties of III-V compounds was predicted in 1952 [8]. Only ten years later in 1962, a red GaAsP laser diode was realized [10]. A plethora of optoelectronic devices, crystal growth and characterization methods soon followed.

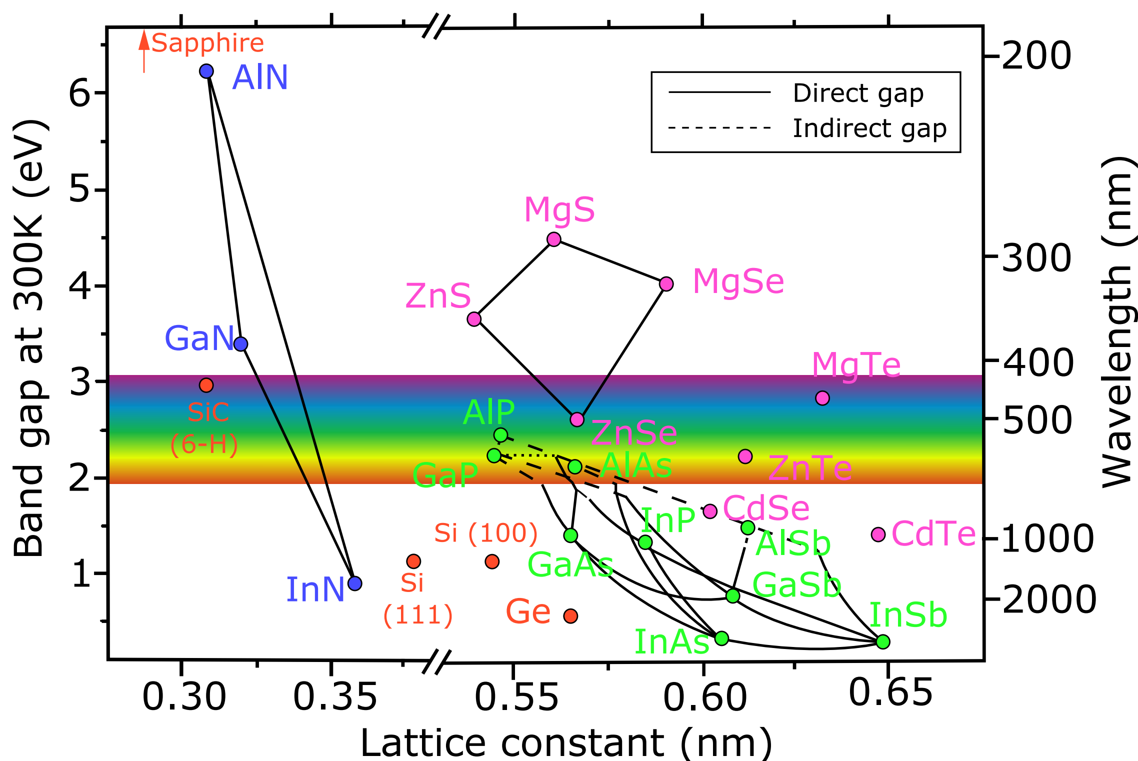


Figure 4: Energy band gaps and lattice constants of semiconductors. The alloy group that the semiconductor belongs to is represented with a colour: III-nitrides (blue), other III-Vs (green), II-IVs (pink) and intrinsic semiconductors (red). The coloured area illustrates the colour of light emitted by the semiconductor. Adapted from reference 20.

Figure 4 presents the various band gaps and lattice constants of most commonly

used III-V semiconductors and other semiconducting material systems. The III-V semiconductors can be alloyed in order to engineer the lattice constant and the band gap almost at will. However, it should be noted that certain alloys are difficult to realize in high quality due to the miscibility gap. Nevertheless, these semiconductor alloys span a wide region in terms of lattice constants and band gaps. Importantly the optical region can be covered from deep UV to near infra red. In addition, other electrical, mechanical and chemical properties of the alloys can differ significantly. Furthermore, the conductive properties can be altered by doping. Thus, p- and n-type materials can be created and typical (opto)electical components realized.

Compared to silicon and other elemental semiconductors, compound semiconductors allow more device applications. Most important is the ability to employ quantum confinement in heterostructures. In a heterostructure, a material region is surrounded by higher band gap material. Therefore, charge carriers can be confined in the low energy region. This local increase of charge carrier density can increase the efficiency of devices. In addition, heterostructures can be employed in field effect transistors (FET). The confinement in addition to doping is used to create two-dimensional electron gas. These transistors exhibit very high electron mobilities as the channel is located in a dopant free region.

Some compound semiconductors show piezoelectric properties. Piezoelectricity can be exploited in the FETs to enhance the creation of the electron gas. It could be possible to create piezoelectric bulk acoustic filters for radio frequency applications. On the other hand, piezoelectricity hinders the performance of optical devices. The piezoelectric potential lowers the spatial overlap of charge carriers in the quantum confined regions, an effect called quantum confined stark effect. The band gap type can be either direct or indirect depending on the semiconductor alloy. In the active area of an optical device, direct band gap is typically chosen.

On the left side of figure 4 are the III-nitride alloys: one subset of the III-V semiconductors (AlN, GaN and InN). These alloys are characterised by a wide band gap together with a good thermal and chemical stability. Therefore, III-Ns are suitable for short wavelength optical applications and high performance electrical components. However, the lattice constant of these alloys differs significantly from other common semiconductor compounds (figure 4). Moreover, the III-Ns preferably crystallize into a wurtzite lattice as opposed to the cubic lattice of most III-V semiconductors. This poses a challenge in manufacturing the III-N alloys as there is a limited amount of suitable substrates.

2.4 Gallium nitride

Gallium nitride (GaN) is a compound semiconductor that belongs to the III-nitride group of III-V semiconductors. GaN has a direct band gap of 3.42 eV at 300 K [2]. This makes GaN suitable for optoelectronic applications, most notably blue LEDs. In addition, the wide band gap results in a high breakdown field. Combined with sublimation point exceeding 1400 °C [2, 21], good thermal conductivity and high electron mobility [2], GaN is an excellent candidate for high performance electrical applications. Indeed, there is increasing deployment of GaN based components in

wireless infrastructure, radar applications and power electronics [6, 7].

Figure 5 presents the crystal structure of wurtzite GaN with one unit cell highlighted. GaN crystallizes either in wurtzite or zinc blende structure, former being more stable and common. Properties of other III-N semiconductors are listed in table 1.

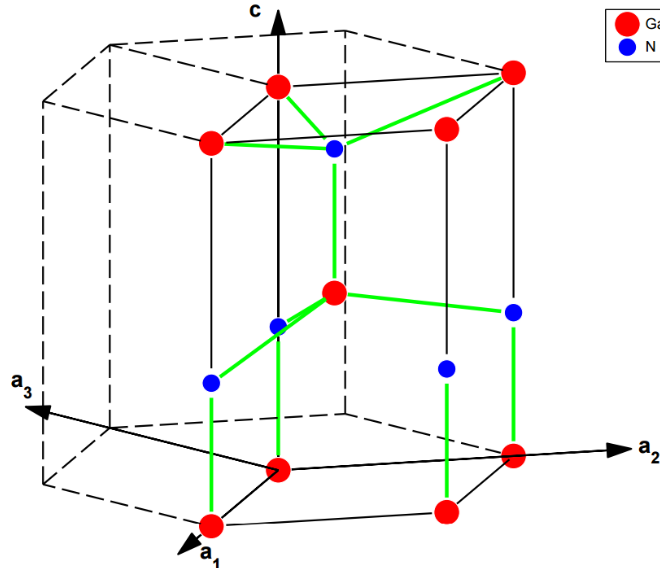


Figure 5: Wurtzite structure of GaN [22].

Table 1: Properties of III-N semiconductors [2].

	GaN	AlN	InN
Band gap 300 K (eV)	3.42	6.2	0.78
Lattice constant a (nm)	0.3189	0.3112	0.3538
Thermal expansion coefficient $\Delta a/a$ $10^{-}6$ $(1/K)$	5.6	4.2	3.2

Wurtzite GaN is a polar material with respect to the [0001] c-axis. Depending on the type of atoms that occupy the lattice sites at the c-planes, GaN is either Ga-polar or N-polar. Figure 5 shows the Ga-polar configuration. In addition, the GaN structure deviates slightly from the theoretical structure. The nearest neighbour distance is about 0.5% larger than the ideal value [2]. In the case of GaN, the nearest neighbour distance is the distance between Ga and N atoms in the c-axis. Therefore, there is an intrinsic electrical field in a GaN crystal. In addition, strain in the crystal causes piezoelectric polarization. However, planes perpendicular to the c-plane, a-plane and m-plane, do not exhibit polarization (figure 6a). Planes angled with respect to the c-plane show some polarization (figure 6b). The polarization

effects can be either detrimental or beneficial for electrical devices depending on the application. Thus, there is a focused research for growing GaN in different orientations [5, 23].

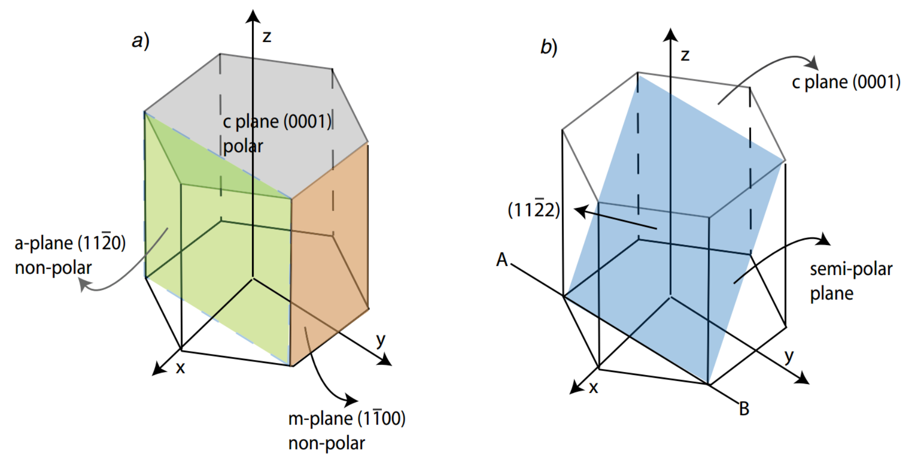


Figure 6: Schematic diagram of a) polar and non-polar crystal planes and b) an example of a semi-polar GaN wurtzite crystal plane [24].

3 MOVPE

In this chapter, metal-organic vapour phase epitaxy (MOVPE) growth is discussed. The principle, growth modes and the growth regime of a MOVPE process are discussed. Finally, MOVPE growth of GaN is considered.

MOVPE is the most commonly used growth method for fabricating compound semiconductor materials on an industrial scale. Other deposition methods exist, such as hydride vapour phase epitaxy (HVPE) or molecular beam epitaxy (MBE), but MOVPE has several advantages over the other technologies. A MOVPE reactor can reach higher growth rates than MBE and, on the other hand, produce higher quality layers than HVPE although at lower growth rates. Furthermore, MOVPE can produce a wide range of material combinations. At present, HVPE is mainly employed for producing substrates, MBE is mainly used for material research purposes and most of commercial devices are processed with MOVPE.

The growth process in MOVPE is based on chemical reactions of organometallic compounds as opposed to MBE where physical deposition (phase transition) is employed. In the case of HVPE, chemical reactions of metal chlorides are used.

3.1 Operation

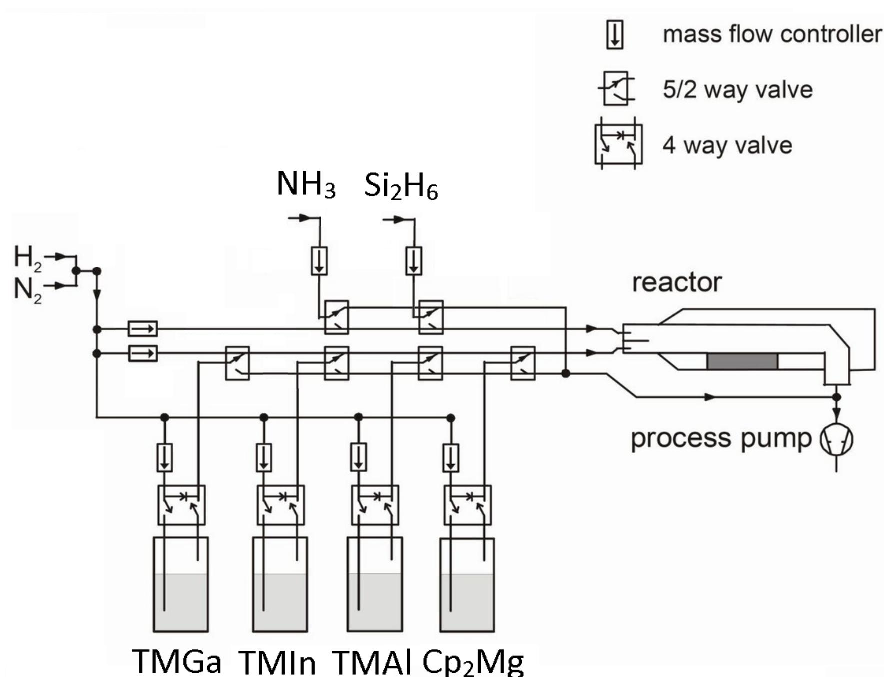


Figure 7: Schematic diagram of the gas lines of a MOVPE apparatus. Adapted from 25.

Figure 7 schematically presents the gas lines in a MOVPE apparatus. Sophisticated gas control is required in order to ensure stable growth rates and, on the other hand, realize step-like material interfaces. Precursor materials are brought

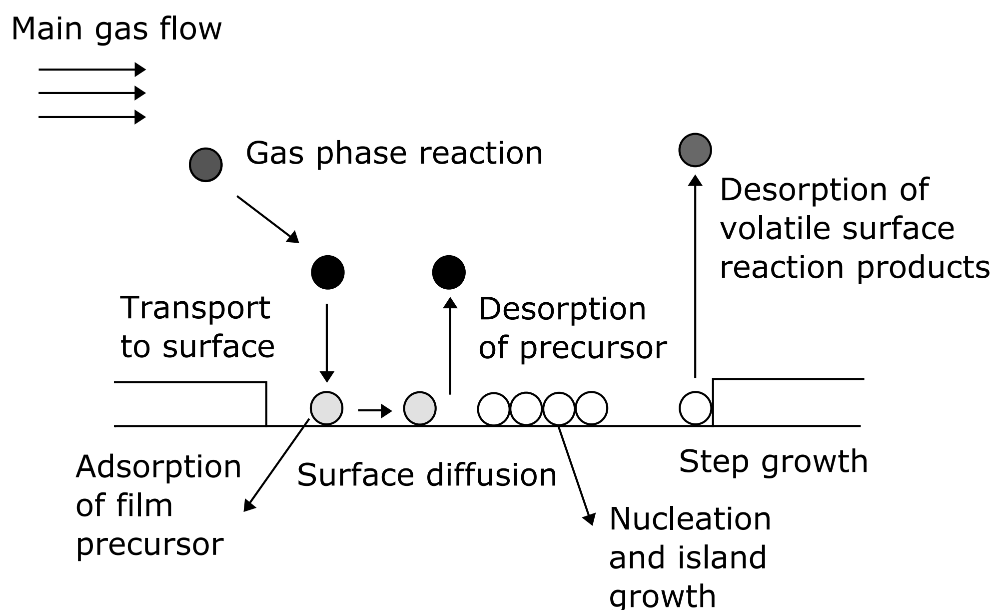


Figure 8: Transport and reaction processes in MOVPE. Adapted from reference 26.

to the reactor in a diluted mixture with a carrier gas, that is usually hydrogen or nitrogen. The carrier gas is used to transport and dilute the liquid phase precursors. The liquid phase source materials are in containers called bubblers. The carrier gas flows through a bubbler and a source material liquid. Some of the source material is absorbed by the carrier gas and, as a result, a saturated vapour is formed. The bubbler temperatures are controlled to obtain suitable vapour pressures. In addition to the host semiconductor materials, dopants are required to fabricate p- and n-type materials.

The reaction chamber is usually made from quartz or stainless steel in order to limit the reactions between reactor walls and gases. In addition, some reactor types have separate inlets for group III and group V precursors to limit parasitic reactions between the precursors, that is, reactions without material deposition.

Growth in a MOVPE reactor is based on chemical reactions of metal-organics, organic compounds and hydrides (figure 8). Inside the reactor there is a heated susceptor that holds the substrate. The growth temperature is in the metastable region of the desired semiconductor material. The precursors decompose on the substrate in a reaction called pyrolysis. The atom in the precursor that will form the desired semiconductor separates from the other precursor molecule atoms. The separated atom diffuses to the substrate where it can be incorporated to the new crystalline layer. The by-products out-diffuse and are removed by the carrier flow. The carrier gas does not participate in the chemical reaction although there can be inadvertent incorporation into the growing layer. Moreover, there is some by-product incorporation, mostly carbon.

Under optimal conditions the formed layer is epitaxial; the grown layer copies the structure of the underlying substrate. The growth conditions promote lateral diffusion on the substrate and nucleation into lattice sites. On the other hand, atoms

that do not bond into lattice sites are desorbed. In addition to deposition, etching of the semiconductor layer can occur depending on the reactant concentrations, temperature, pressure and the type of carrier the gas.

3.2 Growth mode

Three different growth modes can be identified in epitaxy. These are Frank-van der Merwe (FM), Stranski-Krastanov (SK) and Volmer-Weber (VW) growth modes. The dominating growth mode depends on the various ad-atom interactions compared to the ad-atom surface interaction strength. These interactions are affected by the difference in lattice constant of the substrate and the overlayer in equilibrium, electronic hybridization at the interface and accumulated volume strain [27].

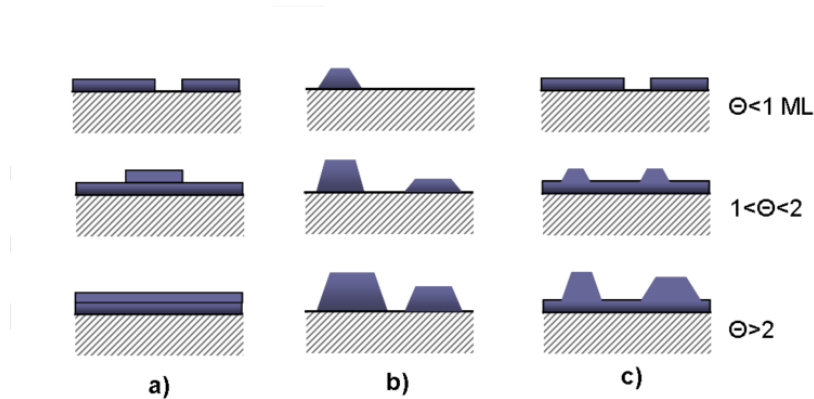


Figure 9: Cross-sectional view of growth modes in thin film growth: a) Frank-van der Merwe, b) Volmer-Weber and c) Stranski-Krastanov. Θ denotes the epitaxial layer thickness in monolayers. [28].

Figure 9 presents the three growth modes. The FM mode is essentially a 2D growth mode, in which each atomic layer is completed before next one begins to form (figure 9a). In the case of the FM growth mode the interaction between the ad-atoms and the substrate dominates. In contrast, the VW growth mode forms islands or aggregates of atoms (figure 9b), because the ad-atom interactions are stronger than the interactions with the substrate. Typically, defects are created to the substrate-island interface to relief strain and these defects propagate to the islands. The VW growth mode can be classified as 3D growth. However, if growth is continued sufficiently long the islands can merge. Unfortunately, structural defects can be created at the interfaces between the islands. On the other hand, the SK growth mode undergoes a transition as the relative contribution between ad-atom and surface adhesive force changes as a function of film thickness (figure 9c). The growth starts with a thin strained 2D layer called the wetting layer. After the critical thickness, 3D islands begin to form on the wetting layer. Opposed to the VW growth mode, the SK mode can relieve the stresses coherently without generating defects

in the substrate-island interface. As with VW growth, the islands can coalescence to a film if growth is sustained.

3.3 Growth regime

Three growth regimes can be identified in typical MOVPE growth process as a function of temperature. These regimes are classified by the dependence of growth rate as a function of temperature and the physical processes causing the differences. At low temperatures (450-550 °C), the growth rate increases with increasing temperature according to the Arrhenius equation

$$V_{growth} \propto \exp \frac{-\Delta E}{RT}, \tag{1}$$

where ΔE, R and T are the energy potential associated to the limiting kinetic process, the ideal gas constant and temperature, respectively. This is know as the kinematic regime. The growth rate can be limited by, for example, the desorption kinetics of CH_3 molecules. Based on equation 1 it can be seen that the growth rate is heavily dependent on temperature. Kinetic regime is typically used for the nucleation layer deposition in the growth of GaN. The low temperature allows adatoms to bind and remain in surface sites with low binding energy. Therefore, the parameter space for material deposition is relaxed. However, the material quality is low.

When the system has sufficient thermal energy, the growth rate is no longer limited by reaction kinetics. Instead, gas phase transport of precursor materials on the surface becomes the limiting factor. This is know as the mass transport limited growth regime, in which the growth rate has a weak temperature dependence

$$V_{growth} \propto \rho D \nabla Y_{MO}, \tag{2}$$

where ρ, D, ∇Y_{MO} are the gas density, diffusion coefficient and the gradient of the metal-organic species mass fraction between the surface and the reactor atmosphere, respectively. The growth is mass transport limited in moderate temperatures, approximately from 550 °C to 850 °C. The temperature dependence can be approximated with the following considerations. Gas density is inversely proportional to temperature

$$\rho \propto T^{-1}, \tag{3}$$

whereas diffusion constant is exponentially proportional to temperature

$$D \propto T^{1.7}. \tag{4}$$

Therefore, the growth rate in mass transport limited growth is weakly dependent on temperature

$$V_{growth} \propto T^{0.7}. \tag{5}$$

The mass transport limited growth rate is not inherently dependent on pressure as gas density is directly proportional to pressure

$$\rho \propto p, \tag{6}$$

and on the other hand, diffusion constant is inversely proportional to pressure

$$D \propto p^{-1}. \tag{7}$$

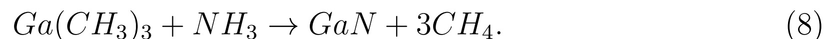
Thus, these two contributions negate each other. However, pressure has an effect on the reaction kinetics and, therefore, can have an effect on the growth rate.

The third growth regime is reached at high temperatures. Typical growth temperatures are over 850 °C. Here, growth can still be classified as being mass transport limited. However, the desorption/etching rate of the surface is significant compared to the growth rate and, therefore, the growth rate decreases with increasing temperature. High growth temperature increases the crystal quality. Ad-atoms that are not bound to high binding energy lattice sites are desorbed. Especially for GaN growth higher pressures and increased H_2 content compared to N_2 or metal-organic species increase the etch rate.

3.4 Growth of GaN

An optoelectronic device can operate efficiently in a wavelength region close to the material band gap. As a result, the III-arsenide and the III-phosphide devices are suitable for wavelengths from the near infra red to yellow light (figure 4). On the other hand, the III-nitride compounds span almost the entire light spectrum (figure 4). Therefore, there has been a large interest to realize III-nitride based optoelectronic devices. Especially efficient blue and green LEDs were sought after. However, growth of epitaxial III-Ns proved to be difficult and the first blue LED based on GaN was demonstrated as late as 1971 [9]. The most serious issues in growth were the crystal quality and the effective doping of GaN.

The chemical reaction producing GaN in a MOVPE reactor can be simply described as



$$Ga(CH_3)_3 + NH_3 \rightarrow GaN + 3CH_4. \tag{8}$$

In this case, one trimethylgallium (TMGa) molecule reacts with one ammonia (NH_3) molecule to produce gallium nitride and three methane molecules. However, the intermediate chemical species and competing reaction pathways are considerably more complex [29]. TMGa and NH_3 are the most common precursors for GaN growth in MOVPE. In addition, triethylgallium (TEGa) and hydrazine (N_2H_4) are sometimes employed as Ga and N precursors, respectively. Hydrogen is typically used as a carrier gas. It should be noted that using nitrogen carrier gas as a precursor is not viable as nitrogen gas is too stable to create atomic species [29]. Nitrogen or mixture of nitrogen and hydrogen carrier gas is employed when growing InGaN-alloys.

GaN growth requires high temperatures, typically over 1000 °C, for high quality. This is due to the fact that the temperature has to be in the metastable region where the material desorption is significant. Thus, incorporation into lattice sites is preferred. Significant sublimation of GaN occurs at over 1000 °C [2, 21]. This temperature can be regarded as the first approximation for the growth temperature. Furthermore, the effective pyrolysis of NH_3 requires high temperatures [29]. At these temperatures, the disassociation pressure of nitrogen from GaN is high. Therefore, high III/V-ratios are used to provide nitrogen rich atmosphere. High nitrogen concentration limits the decomposition of the crystal.

Typical dopants are disilane (Si_2H_6) and bis-cyclopentadienyl magnesium (Cp_2Mg) for n-type and p-type GaN, respectively. One of the challenges of device fabrication is the low quality of p-type GaN. As-grown Mg-doped GaN shows high resistivity. Thermal activation of Mg dopants is required to realize p-type material. The Mg acceptors are passivated by hydrogen during growth. Even after annealing, the resistivity of p-GaN is high and on the other hand the hole concentration is low. Conversely, the conductivity of n-type GaN is about two magnitudes higher. The poor characteristics of p-type GaN are due to the high activation energy of Mg acceptors in the crystal. The activation energy value is about 160-200 meV [2, 30]. Thus, at room temperature only 6% of the acceptors are activated [30]. Other group II elements have been studied for p-type doping. However, it seems that although Mg doping is not optimal, the alternative dopants studied do not improve the electrical properties due to poor solubility or activation energy [2, 30].

3.5 Substrates for GaN epitaxy

The lack of high quality native substrates is a serious obstacle in epitaxial growth of III-nitrides. Whereas substrates for phosphide and arsenide compounds (eg. GaAs, InP) can be grown using standard Czochralski or Bridgman-Stockbarger processes, melt based growth of III-nitrides is not viable. There are two main causes for this. Firstly, the melting points of III-nitrides are high. For instance, the theoretical melting point of GaN is 2500 °C [2]. Furthermore, the disassociation pressure of nitrogen at that temperature is estimated to be 45 000 atm [2]. Therefore, it is clear that GaN melt cannot be created at least without extreme conditions.

GaN is widely grown on non-native substrates, although native ammonothermally grown substrates exist [11]. However, native substrates are not available at high quality and sufficient sizes. Sapphire, Si and SiC are the most used substrates for epitaxial growth of GaN. The use of these substrates presents challenges especially in lattice mismatch, thermal expansion mismatch and, in the case of silicon, chemical stability. It is evident that the substrate choice is a compromise between factors such as price and lattice mismatch together with electrical, chemical and mechanical properties.

Early experiments of GaN growth were performed on sapphire substrates. C-plane (0001) sapphire (Al_2O_3) is somewhat compatible with c-plane GaN despite the considerable 13.9% lattice mismatch and moderate thermal expansion coefficient (34%) mismatch. However, by employing an AlN interlayer and using coincidence

site epitaxy, high quality GaN layers can be realized. Sapphire presents a challenge for device processing as an insulating substrate. Either contacts have to be deposited on the front side of the wafer or the wafer has to be removed. Moreover, the thermal conductivity of sapphire is low compared to Si or SiC. From this point of view, sapphire is not a good candidate for high performance applications. However, the high electrical resistivity can improve the breakdown field of the device in power applications. The price of sapphire substrates is moderate, between silicon and SiC.

SiC substrate offers some of the best properties for GaN growth. From a growth perspective, SiC offers low lattice (3.5%) and moderate thermal expansion coefficient (25%) mismatch. On the other hand, SiC has high breakdown field and high thermal stability. SiC has a sublimation temperature of 2730 °C [5]. In addition, SiC has higher thermal conductivity than sapphire or Si. These properties make SiC an excellent substrate for high performance applications. However, manufacturing of high quality SiC substrates is difficult and expensive. As with GaN bulk substrates, melt based processes can not be used. Moreover, over 4-inch wafer sizes are not yet available at suitable quality. This increases the chip cost as processing price for a wafer is more or less the same but there are less chips per wafer. Thus, SiC substrates are commonly limited to high end components. However, III-N component manufacturers have found niches for their products. For example, a range of LEDs on cheap silicon substrates to high performance SiC variants are available.

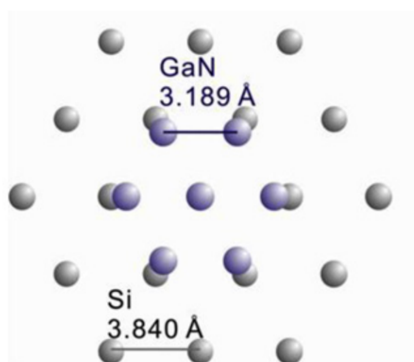


Figure 10: Superimposed atomic arrangements of a (111) oriented silicon substrate and a c-plane of wurtzite GaN lattice. Adapted from reference 23.

Silicon is the newest widely adopted substrate choice for GaN growth. Although silicon substrates are extensively used in microelectronic industry, the adoption for GaN growth has been challenging. Major challenges arise from the mechanical and chemical differences between Si and GaN. Nevertheless, silicon substrates for III-N devices have received increasing interest. High quality Si substrates are available up to 12-inch size. GaN is commonly grown on (111) oriented silicon substrates. Although at this time only 8-inch (111) oriented silicon substrates are widely available. Figure 10 presents the atomic arrangements of silicon cut along (111) plane and c-plane of wurtzite GaN. It can be seen that the atomic configurations are compatible. However, there is a considerable lattice mismatch (17%) and large thermal expansion mismatch (46%) between Si and GaN [13]. MEMS processing on (111) oriented

silicon substrates is fairly typical meaning that substrates are available at low cost, although microelectronics industry prefers (100) orientation. Furthermore, processing tools for silicon substrates are readily available. In addition, it is suggested that some obsolete silicon device processing facilities could be re-purposed for GaN on Si power electronics processing. Integrating GaN based electronics with Si-CMOS is a promising long term goal. It might be possible to exploit the piezoelectricity of GaN to create acoustic wave filters for radio applications [31].

4 Aixtron 1x6" CCS MOVPE

The Aixtron 1x6" close coupled showerhead (CCS) MOVPE apparatus is configured for III-nitride growth on 6-inch wafers. This reactor has some modern features targeted for III-nitride growth on silicon wafers such as a multi-zone heater and extensive in-situ monitoring. This chapter considers the system characteristics and in situ instruments.

4.1 System

The apparatus has a radial flow reaction chamber where the precursors are introduced perpendicular to the substrate and are evacuated at the edges. Figure 11 presents the flow channels in the reactor lid. There are two plenums on top of the substrate from which III and V group precursors are provided. There are two separate flow channel arrays in close proximity to the wafer, an arrangement resembling a showerhead. Some flow channels on the showerhead can be used as optical windows for in situ monitoring. The system is a cool wall reactor; the showerhead is cooled by water flow. The design is intended to limit the parasitic reactions that can be significant in III-N material growth. Firstly, mixing of the precursors takes place in the reaction chamber. Furthermore, the pyrolysis reactions occur at the substrate surface. In addition, the CCS scheme improves uniformity.

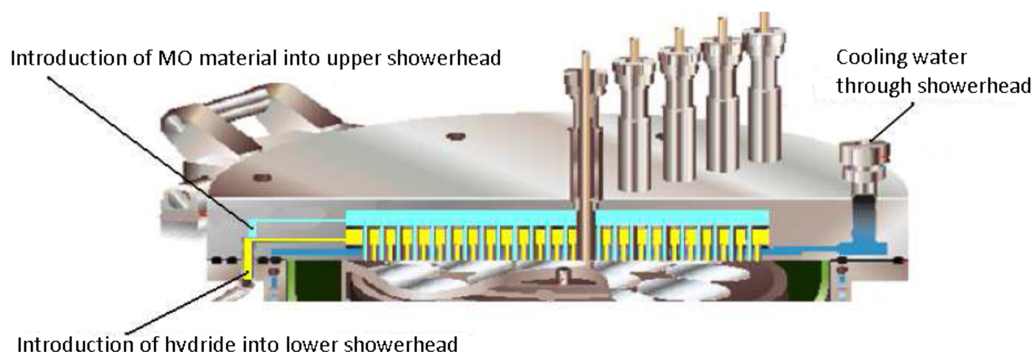


Figure 11: Close coupled showerhead reactor lid of the Aixtron MOVPE apparatus [32].

The substrate is placed on a SiC coated graphite susceptor. The SiC coating is used to improve thermal and chemical stability of the susceptor. The susceptor rotates in order to provide uniform temperature profile and precursor concentration. The susceptor is heated from underneath using three tungsten coils. The arrangement of these coils is presented in figure 12. The coils form three radial zones. These zones can be utilized to fine tune the radial temperature profile of the susceptor. This is beneficial as the substrate bows during growth. Therefore, the substrate surface temperature and bowing can be controlled.

The reactor provides two temperature values. The first value is the susceptor temperature. This value is measured with thermocouple that is located under the

susceptor in a close proximity to it. The second value is given by the in situ measurement setup which is discussed in the next chapter. The in situ measurement setup monitors either the susceptor surface temperature or the wafer surface temperature depending on whether there is a wafer in the reactor. It should be noted that the difference between the thermocouple temperature value and the measured wafer surface temperature can be over 200 °C during growth.

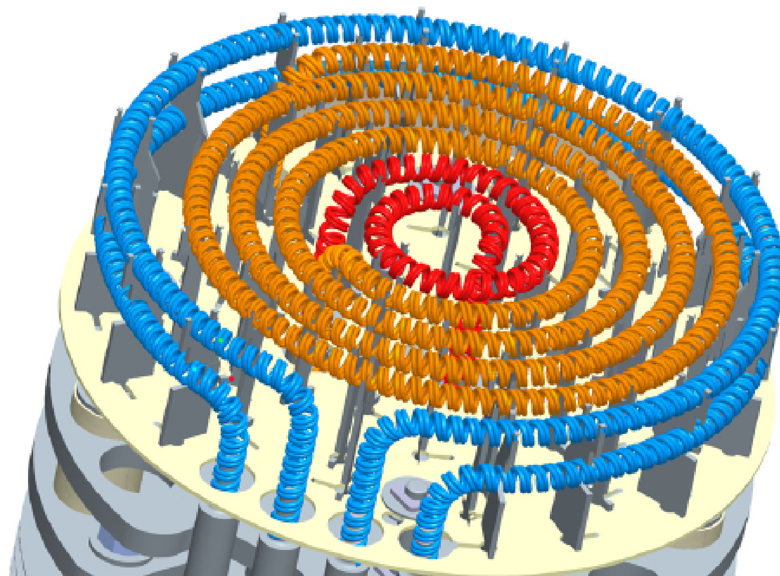


Figure 12: Three susceptor heater zones of the Aixtron MOVPE apparatus [33].

Thermal control is especially important as the substrate size is increased. Larger substrates are more prone to cracking because the thermal and mechanical stresses are more pronounced. In addition, III-nitride growth is characterized by lattice and thermal mismatches between the substrate and the epitaxial layers. Moreover, the incorporation of indium in the InGaN alloy is extremely dependent on temperature. Therefore, strain engineering and thermal control are vitally important.

4.2 In situ monitoring

In situ monitoring of the growth process has become vital for high quality material growth by MOVPE. These type of instruments provide better insight about the conditions during growth, thus allowing better optimization of the growth process. In addition, as growth conditions vary, some critical processing steps might require active recipe control. For example, in the case of GaN on sapphire, nucleation has major impact on the epitaxial layer quality. Therefore, nucleation could timed using reflectance of the surface to ensure appropriate formations. In situ monitoring allows to fabricate more delicate structures and, on the other hand, reduce variance between growth runs.

In some cases, in situ monitoring can reduce the need for other characterization equipment. As there may not be a need to employ an external tool, process

development can accelerate. In addition, it can be more accurate to characterize the individual layers as they form as opposed to extracting information from the complete film stack. However, characterization tools such as x-ray diffraction and Hall measurement are usually required. Nevertheless, the data provided by in situ monitoring could be correlated with that obtained by other characterization tools. In this case, some samples would be characterized with the external instruments.

Typical in situ measurements include layer thickness, wafer curvature and surface temperature measurements. The measurements are usually conducted optically. Physical contact with the substrate is usually not possible due to high temperatures, pressure gradients and delicate gas flows. Flow ports on metallic wall reactors can be employed as optical paths. On the other hand, instrument placement on quartz reactors can be easier.

Reflectance measurements can be utilized to assess surface morphology and film thickness. The thickness measurement is based on simple Fabry Perot oscillations. A laser beam is reflected from the sample surface and focused to a detector. Layer thickness (growth rate) can be resolved from the period of the oscillations. In addition, material quality and composition can be estimated based on the oscillation amplitude. More information on the film properties can be extracted by fitting a simulated curve to the measurement.

The reflected intensity is a sum of the reflection from the film surface and interferences inside the film stack. Considering a simple one layer model with a absorbing substrate, the reflectance has a maximum when the path difference equals an integer multiple of the wavelength

$$2nd = m\lambda, \quad m \in \mathbb{N}, \tag{9}$$

where n is the refractive index of the film, d is the film thickness and λ is the wavelength. Similarly, the reflectance has a minimum when the path difference is equal to an integer multiple plus half wavelength

$$2nd = (m + \frac{1}{2})\lambda, \quad m \in \mathbb{N}. \tag{10}$$

The reflectance at the air film interface is given by

$$R = (n-1)^2 + \frac{k^2}{(n+1)^2} + k^2, \tag{11}$$

where n and k are the refractive index and extinction coefficient of the film, respectively.

Figure 13 schematically presents three cases of in situ reflectance measurement. Ideal growth is characterized by constant amplitude and stable average reflectivity (figure 13a). Slight growth rate variations under the measurement area cause the reflectivity amplitude to decrease while the average reflectivity stays constant (figure 13b). On the other hand, increasing surface roughness decreases the average of the reflectivity (figure 13c). It should be noted that these two unideal cases are not mutually exclusive.

The MOVPE apparatus used in this work has Laytec Epicurve TT in situ measurement setup. Reflectance is measured at three different wavelengths, 405 nm, 633 nm and 950 nm. Three lasers are focused at normal incidence on the subsrate through optical ports on the showerhead. The reflectance can be measured at different spots along the same radius as the susceptor rotates.

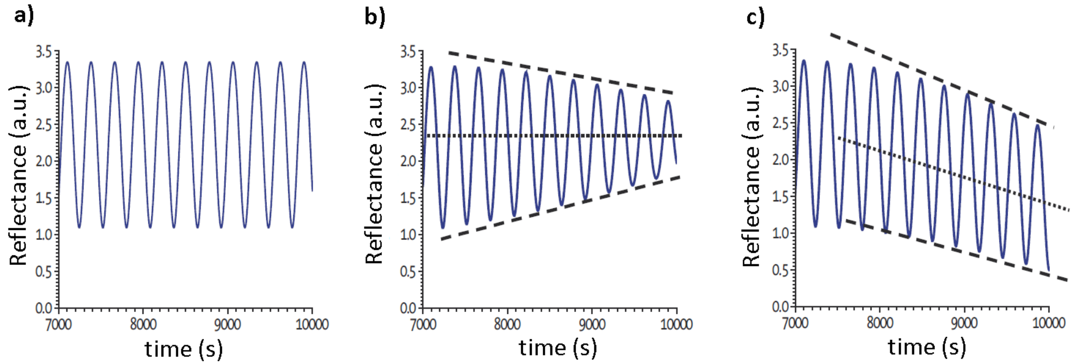


Figure 13: Three cases of wafer surface evolution based on in situ reflectance measurement: a) ideal growth, b) growth rate variations and c) increasing surface roughness [34].

Wafer curvature measurement has become important as wafer sizes have increased. There are mainly two reasons. Firstly, the change in wafer curvature allows to have an estimate of the stresses on the substrate and epitaxial layers. On the other hand, tolerances for wafer bow in processing have become more strict as wafer size is scaled up.

Figure 14 schematically presents optical wafer curvature measurement. The Epicurve TT measures the wafer curvature by focusing two parallel 405 nm wavelength laser beams on the substrate at normal incidence. The reflected beams are directed to a CCD array. The deviation of the laser spots on the CCD array is then converted to an estimate on the wafer curvature. In the case of a flat wafer, the spot separation stays constant (figure 14a). On the other hand, concave (convex) curvature causes the separation to decrease (increase), figure 14b (c).

Figure 15 presents three factors for wafer curvature change. Temperature gradients will bend the wafer as thermal expansion affects the wafer non-uniformly. In figure 15a, the wafer back temperature is higher than the wafer surface temperature. Thermal expansion causes concave wafer bow. This is typical for heated susceptor reactors. In figure 15b, lattice mismatch induces stresses between the layers. On the left (right) side, epitaxial layer that has greater (smaller) lattice constant than the substrate is grown. The stress induced causes convex (concave) wafer bow. Finally, layers with different thermal expansion coefficients experience thermal stress when the temperature is varied (figure 15c). On the right (left) side the lower (upper) film has higher thermal expansion coefficient. The film stack temperature is increased and concave (convex) wafer bow is observed. It should be noted that the wafer curvature and temperature profile are connected as the wafer contact to the susceptor changes with varying wafer curvatures.

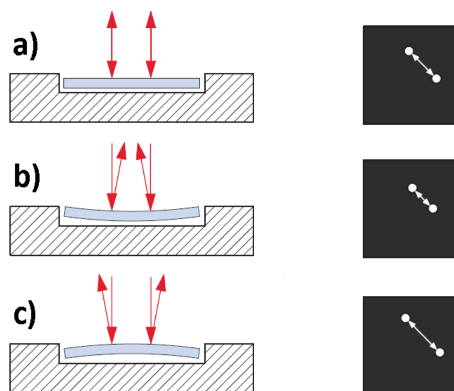


Figure 14: Optical in situ wafer curvature measurement. The wafer on the susceptor and the paths of the laser beams are shown at left and the laser spots on the CCD array at right for a) flat, b) concave and c) convex wafer. [34].

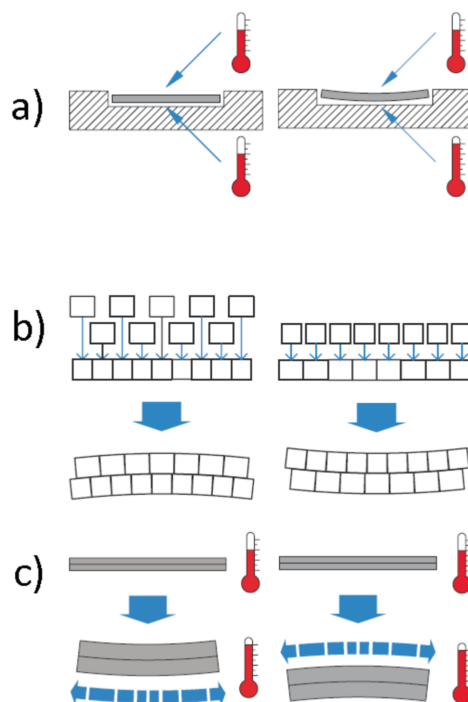


Figure 15: Effect of a) thermal gradient, b) lattice mismatch and c) different thermal expansion coefficients of layers on the wafer curvature [34].

The surface temperature of the wafer is obtained by fitting a black body radiation curve to the infra-red emission of the wafer. The measurement can be conducted either using two or more detectors with different band pass filters or with one CCD detector. In the case of the CCD detector, the emission spectrum is split with a

prism. In both cases, relative intensities of certain wavelength regions are used. For accurate measurements the wafer emissivity is estimated. Emissivity is the difference between ideal black body radiation and the measured object. Emissivity is greatly affected by the film stack thickness and composition.

The reactor used in this study has two types of wafer temperature measurement systems, Aixtron ARGUS and Laytec EpiTT. ARGUS uses an array of diodes to map the whole wafer as the wafer rotates. The diode array measures the wafer emission on two wavelengths. On the other hand, EpiTT provides emissivity corrected temperature on certain locations with the same radius on the wafer. The measurement is based on the CCD array approach. In addition, a LED light source is used to measure the wafer reflectivity spectrum in the infra-red for the emissivity correction. An optical fibre is connected between the reactor showerhead and the instrument. In principle, emissivity corrected wafer temperature mapping is possible. However, it could prove difficult to connect multiple CCD array based instruments to the reactor. In practice, the EpiTT is used to ascertain the growth temperature. On the other hand, ARGUS is employed to adjust heater balance for uniform wafer temperature profile.

Stable and uniform wafer surface temperature is vital in delicate growth steps. For instance, indium incorporation in InGaN quantum well formation for LEDs is extremely sensitive to growth temperature. In addition, uniform radial temperature profile can help to minimize wafer bow and film stresses during growth.

Additional information can be extracted when multiple in situ measurements are combined. For example, the temperature gradient of the substrate or the layer composition can be estimated [35]. The composition analysis requires information on the wafer surface temperature, wafer curvature and layer thickness. The change of curvature as a function of layer thickness can be used to assess the lattice mismatch between the substrate and the epitaxial layer. The lattice mismatch can be then in turn used to estimate the composition of the epitaxial layer. In addition, deviation from linear relation between thickness and curvature can be seen as a change in the material quality. For example, a transition to a different curvature slope might indicate the onset of plastic deformation or relaxation of the epitaxial layer [35]. Therefore, critical thickness for certain films could be obtained.

5 Characterization methods

Characterization is required in order to assess material quality and properties. The results can be then in turn used to optimize growth parameters. Modern MOVPE reactors offer some in situ monitoring. However, wafer mapping or more delicate measurements, such as x-ray diffraction, cannot be conducted during growth. In this chapter, optical epitaxial layer thickness measurement with spectrophotometer, x-ray diffraction and wafer geometry measurements are discussed. These measurements provide insight about the epitaxial growth uniformity, material quality (dislocations), wafer strain and bow. Other typical measurements are photoluminescence for quantum well uniformity assessment and Hall measurement for electrical properties such as mobility.

5.1 Spectrophotometer

Spectrophotometer is a measurement tool for optical characterization of thin film structures. The tool employs normal incident white light spectroscopy to simultaneously estimate film thickness and optical properties. A simple one layer model for white light reflection gives a thickness estimate

$$t = \frac{N}{2n(\frac{1}{\lambda_1} - \frac{1}{\lambda_2})}, \tag{12}$$

where t, N, n, λ_1 and λ_2 are thickness, number of oscillations between two reflection maximums, refractive index of the film and the wavelengths of the maxima, respectively.

For more accurate measurements, wavelength dependent refractive index and absorption coefficient together with multiple layers are employed [36]. Absolute reflectivity can be resolved by comparing the sample reflectance spectrum to a know reference. A simulated reflectance is fitted to the experimental curve to extract material parameters.

In this work, the GaN on Si structure was modelled as a two layer system in order to measure the film thickness. It should be noted that the film stack consists of an AlN layer, an AlGaN graded buffer and two GaN layers. The measurement software provided a table of the refractive index for the silicon substrate as a function of wavelength. The epitaxial layers were modelled with a two coupled Lorentz oscillator model, the dielectric constant [36]

$$\epsilon(E) = \epsilon_\infty (1 + \sum_{j=1}^{2} \frac{A_j^2}{(E_{center})_j^2 - E(E - iv)}), \tag{13}$$

where ϵ_∞, E_{center}, A_j and v are the high frequency lattice dielectric constant, the center energy of each oscillator, the amplitude (strength) of each oscillator and the electron scattering frequency, respectively. Table 2 presents the parameters used in the model. The coupled model is a generalization of the standard Lorentz oscillator model. In the standard model, the oscillators are independent.

Table 2: Parameters used in the coupled Lorentz oscillator model.

Oscillator	ϵ_∞	$E_{center}(eV)$	$A_j(eV)$	$v(eV)$	coupling coef.
1	3.278	5.716	3.605	0.2826	2.874
2	3.278	4.226	1.325	0.8025	-

Despite the fact that the film stack was modelled with a two layer system, the tool produced accurate measurements. The results were confirmed by imaging a cross-sectional sample of the epitaxial layers with scanning electron microscope.

5.2 X-ray diffraction

X-ray radiation is electromagnetic radiation with wavelengths between gamma rays and ultraviolet light. Typically, x-rays are generated by bombarding a metal with electrons in a vacuum tube. X-rays can be used to study the material lattice as the x-ray wavelength is comparable to the atomic spacing enabling x-ray diffraction (XRD) measurements [37]. Compared to electron microscopy or atomic force microscopy, the x-ray based characterization has a larger probe size. The diffraction based method sees the collective effect of crystal quality whereas the microscopes can see only individual defects.

The wavelength in diffraction studies is in the order of 0.1 nm. The crystal lattice can be seen as a diffraction grating. Constructive interference occurs when the path difference from the lattice planes is equal to an integer multiple of wavelength. The constructive interference is described by the Bragg's law

$$n\lambda = 2dsin\theta, \tag{14}$$

where n, λ, d, and θ are the order of diffraction, wavelength, distance between the lattice planes and angle of diffraction, respectively. Figure 16 presents the Bragg's law geometrically. In practice, n is chosen to be one. This can be done by using specific lattice planes. The distance between the planes can be altered by using a subset of lattice plane group, for example, taking every other lattice plane. For a

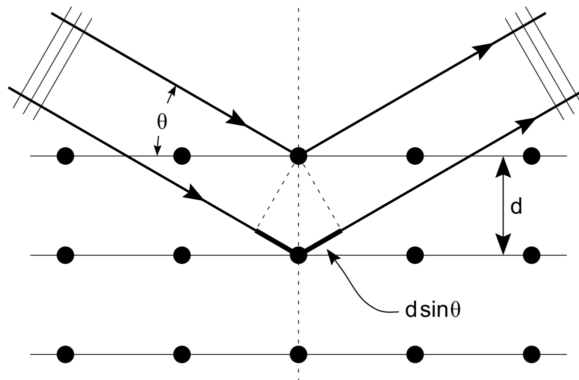


Figure 16: Geometrical representation of the Bragg's law [38].

hexagonal lattice, the plane spacing is [39]

$$d = \sqrt{\frac{3}{4(\frac{h^2+k^2+hk}{a^2} + \frac{3l^2}{4c^2})}}, \tag{15}$$

where h, k and l are the Miller indices of the plane and a and c are the lattice constants.

Figure 17 presents a typical high resolution x-ray diffraction (HRXRD) -setup. The output beam of a x-ray source is directed to a monochromator. The monochromator is used to select ideally a single wavelength from the beam and, on the other hand, make the beam narrow. The monochromator is based on quadruple diffration from nearly perfect germanium crystals [15]. This increases the the resolution of the setup as the Bragg's condition is satisfied at smaller range. The incident beam angle from the sample surface is called ω. The sample diffracts the incoming beam. The angle between the diffracted beam and the incident beam is called 2θ. The diffracted beam is then directed to a detector through an analyser crystal. Similar to the monochromator, the analyser increases the measurement resolution. The analyser employs three diffraction events. Thus, the acceptance angle to the detector is reduced. However, when using the monochromator and the analyser the measured intensity drops. As as result, HRXRD measurements are typically slower than conventional XRD measurements. Therefore, the setup choice is a compromise between time and precision.

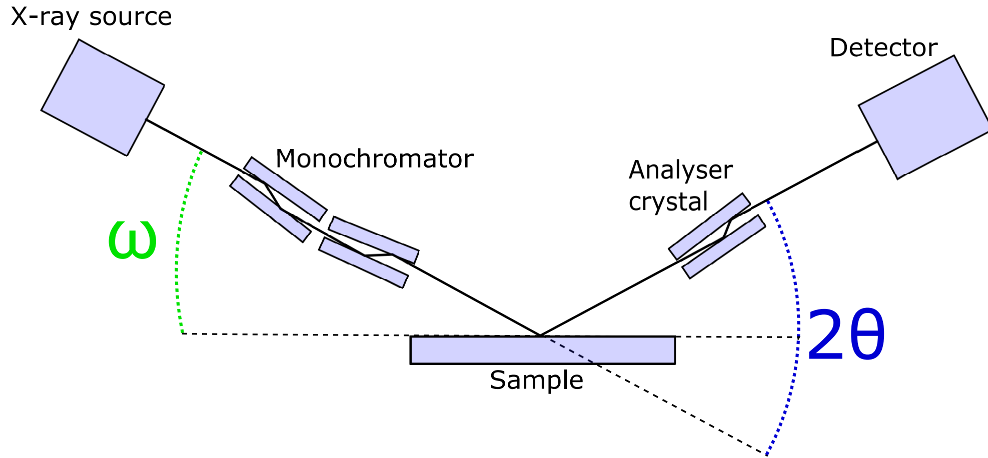


Figure 17: Schematic diagram of high resolution XRD setup.

The concept of reciprocal space is convenient when processing diffractions from lattice planes. Reciprocal lattice can be constructed from the basis vectors of three dimensional lattice. If the direct space lattice vectors are $\mathbf{a}_1$,$\mathbf{a}_2$ and $\mathbf{a}_3$, the reciprocal

space vectors are defined as

$$\mathbf{b}_1 = \frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3},$$
$$\mathbf{b}_2 = \frac{\mathbf{a}_1 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3} \text{ and} \tag{16}$$
$$\mathbf{b}_3 = \frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3}.$$

It can be seen that the cross product in equations 16 causes the reciprocal lattice vector to be perpendicular to the respective real space vectors. In addition, the denominator of the equations is the volume of the real space unit cell. Therefore, reciprocal lattice unit cell volume is the reciprocal of the real space volume. These properties lead to the usefulness of the reciprocal space. It turns out that if a vector $\mathbf{H}_{hkl}$ is drawn in the reciprocal space from the origin to coordinates (h,k,l), the vector is perpendicular to the real space lattice plane with Miller indices (hkl). The length of the vector $\mathbf{H}_{hkl}$ is related to the plane distance in real space, $|\mathbf{H}_{hkl}| = 1/d_{hkl}$. Furthermore the vector $\mathbf{H}_{hkl}$ is related to the wave vectors of the incident and scattered beam, $\mathbf{H}_{hkl} = \mathbf{k}_0$ - $\mathbf{k}_s$. [15]

Two type of measurements are typically conducted when characterising semiconductor samples [37]. These are the ω and the $\omega - 2\theta$ scans. The $\omega - 2\theta$ scan can be seen as changing the length of the scattering vector in reciprocal space while maintaining the direction. The ratio between the angles is maintained, that is, $\omega = 2\theta/2$. This essentially means that lattice planes of the same orientation but with different spacing are probed. Individual peaks around a certain reciprocal lattice point are typically created by different materials in the sample. Peak broadening on the other hand is mostly caused by the variation in the lattice spacing. The ω scan, on the other hand, traces an arc around the origin of reciprocal space. The scattering vector length is maintained but the direction is changed. This can be interpreted as probing lattice planes with the same spacing but with different orientation. The peak broadening can be related to material quality.

Reciprocal space maps are 2D slices of the reciprocal space. Typically, multiple ω scans are conducted with different $\omega - 2\theta$ values. Reciprocal space maps are especially useful for characterising strained layers. The reflection peaks in these samples can have considerable ω offsets. The individual layer quality can be estimated based on the ω and $\omega - 2\theta$ peak broadening. In the reciprocal space, these are the Q_x and Q_y coordinates. The relaxation between the layers can be seen in the separation of the peak maxima in ω-axis. Similarly, relaxation can be seen in the peak separation in terms of the Q_x coordinate. The incident and scattered beam angles can be translated to reciprocal spaces using the equations [40]

$$Q_x = \frac{1}{2}(cos(\omega) - cos(2\theta - \omega)) \ and \tag{17}$$

$$Q_y = \frac{1}{2}(sin(\omega) + sin(2\theta - \omega)). \tag{18}$$

The structure of a highly non-ideal crystal film is typically approximated with the mosaic model [41]. It should be noted that for lower defect densities other models should be employed [37]. The mosaic model assumes that the film consists of ideal grains that are slightly misoriented with each other. The misorientation is divided into two orthogonal components. Rotation around the axis perpendicular to substrate surface is called twist and rotation parallel to substrate is called tilt. At the grain boundaries, tilt creates edge dislocations. On the other hand, twist causes screw dislocations.

The assessment of material quality based on XRD measurements is not trivial. Although the broadening of diffraction peaks can be related to material quality, there is a plethora of other factors. In addition, the choice of the defect model has a considerable effect on the estimates produced. However, XRD measurements are typically employed to assess a sample series quantitatively. Then one can assume that most of the differences are caused by the samples and less by the measurement setup. The qualitative analysis, for example, between different research groups, is considered somewhat unreliable. The XRD line shapes can be affected by dislocations, strain, wafer curvature, thickness variation, composition variation, limited sample size and measurement setup [37]. However, for high dislocation density samples, the effect of material quality dominates. This is usually the case for GaN layers on silicon substrates. In addition, some of the effects can be separated by taking scans from different diffraction planes [37, 42].

5.3 Wafer geometry measurement

Wafer geometry measurements are conducted to assess the strain of the epitaxial layers after growth. In addition, wafer bow is crucial as too high bow can prohibit post processing. Non-contact measurement is usually required in order to limit wafer contamination.

In this study, a non-contact wafer geometry measurement was used. The measurement is based on capacitance change. A capacitance probe is brought to close proximity to the wafer. The capacitance between the wafer surface and the probe as a function of distance is known [43]. The measured capacitance is compared to a capacitance of a known reference. Thus, the distance can be calculated.

There are probes on either side of the wafer. When the distances between the probes and the wafer are measured, the wafer thickness can also be estimated. The wafer is scanned with the probes and, thus, the wafer geometry can be resolved.

The probes employ a so called push-pull scheme. A probe contains two terminals and an AC current is run between the terminals. This configuration limits the effect of varying wafer conductivity on the measurement [43].

6 Gallium nitride on silicon

Epitaxy of GaN on Si is challenging because of the vastly different material properties. Firstly, the lattice mismatch of c-plane GaN and (111) Si is 17% [2]. Second reason is the 46% difference in the thermal expansion coefficients between the two [2]. Moreover, GaN cannot be directly grown on silicon because gallium reacts aggressively with silicon causing a phenomenon called meltback etching [5]. Despite these challenges, (opto)electronic grade GaN can be realized on silicon substrates. Considerable amount of research has been directed to match GaN and Si [5]. Indeed, multiple seed and buffer layer schemes have been proposed [5].

From the device perspective, the high resistivity of Al containing layers and, on the other hand, Si substrate conductivity and low breakdown field place limitations [5]. Moreover, in optical applications, the Si substrate absorbs considerable amount of GaN emitted light. Therefore, the silicon substrate has to be removed [23]. Nevertheless, commercial GaN on Si blue LEDs are available [23].

6.1 Substrate orientation

The (111) cut silicon is by far the most used orientation for GaN on Si devices. There are two main reasons. First, silicon cut along this axis has a hexagonal symmetry on the surface. The atomic arrangement is similar to the c-plane of GaN albeit the lattice constant is different (figure 10). Therefore, a buffer layer has to account for matching these two lattices. Secondly, (111) oriented substrates are widely available up to 8-inch wafers. On the other hand, GaN can be grown other silicon orientations as well such as (100) or some other more exotic planes. However, in the case of the 100 orientation, GaN can easily form multicrystalline film [44]. This occurs because r-plane GaN, the typical orientation on (100) Si, can grow on four different alignments. The substrate symmetry has to be broken to favour one orientation, for example, using wafer miscut [44]. The (100) silicon would be preferred for integration with Si-CMOS. In addition, (100) substrates are available up to 12-inch size.

The more exotic growth planes typically require substrate patterning. Processing steps before the epitaxial growth usually render the fabrication scheme economically unviable [23]. On the other hand, these substrates could allow to grow GaN on other orientations than the typical c-plane. GaN is a polar semiconductor as discussed in chapter 2.4. Therefore, some device applications can benefit from different internal electric fields. For example, a HEMT structure exploits the piezoelectricity to create the electron gas channel. On the other hand, piezoelectricity induced quantum confined stark effect lowers the LED efficiency.

The substrate can be patterned to reduce the dislocation density. Typically SiO_2 or Si_3N_4 mask is deposited on the substrate. Then, photolithography and etching is used to expose windows of silicon. The initial growth conditions are set so that pyramid shaped GaN form in the mask windows. The layer is then coalesced by lateral growth. The lateral growth should bend the threading dislocations in plane and cause them to annihilate [5, 23]. This scheme is called epitaxial lateral over-

growth (ELOG). Another approach is to etch holes or slots to the substrate. In this case, the strain should be relieved by the voids left in the layer interface. Therefore, the generation of dislocations should be inhibited [23]. These two approaches have been shown to reduce the amount of dislocations. However, dislocations are created to the island interfaces during the coalescence. Local strain can be high in the interfaces, leading to cracks. Unfortunately, the benefit of these methods is typically overshadowed by the increased processing cost [5, 23].

6.2 Buffer layers

As with most metals, gallium diffuses into silicon at elevated temperatures. Unfortunately, gallium and silicon form an alloy at high temperatures in a phenomenon called meltback etching. It is postulated that the presence of nitrogen accelerates the reaction [5]. The process is not self limiting and can render the whole wafer surface unsuitable for growth. Therefore, an intermediate layer is is required between the silicon substrate and the GaN layers.

Proposed seed layers include converting some of the wafer surface to SiC and AlAs or AlN seed layers [1]. The seed layer has to be sufficiently thick and have reasonable quality so that gallium cannot diffuse to silicon through cracks or pits in the layer. On the other hand, compatibility with layers to be grown on top of the seed layer is beneficial for crystal quality. The seed layer quality defines a starting point for the subsequent layers. It has been discovered that appropriate AlN nucleation layers can be readily grown on silicon. Indeed, the AlN nucleation layer is the most employed solution in GaN on Si device growth.

6.3 Wafer bending

While the dislocations in the GaN layer are limiting device performance, the large difference in thermal expansion is in fact more severe a limitation. Indeed, it is difficult to grow sole GaN layers with thickness in excess of 1 μm. When cooling down a GaN film on Si after growth, tensile stress on the GaN layer is created. Sufficiently strong tensile stress can cause the wafer to crack. Moreover, meltback etching can occur if cracks are created during the growth. Therefore, epitaxy of GaN on Si is essentially strain engineering. The GaN layer is compressively prestrained during growth. Ideally, the compressive pre-straining and tensile thermal stress negate each other at room temperature. In addition, the wafer curvature should be within specifications for post processing.

Figure 18 presents two buffer layer schemes for strain engineering. The buffer layer needs to deal with interplay of multiple factors. These include the interface to the nucleation layer, strain engineering and dislocation annihilation. In addition, some electrical and optical considerations are required depending on the device structure. It can be seen that in the III-nitrides AlN has the smallest lattice constant followed by GaN and InN (Figure 1). Therefore, buffer structures containing AlN create some compressive strain for pseudomorphic GaN. This in turn helps to counteract the tensile thermal strain.

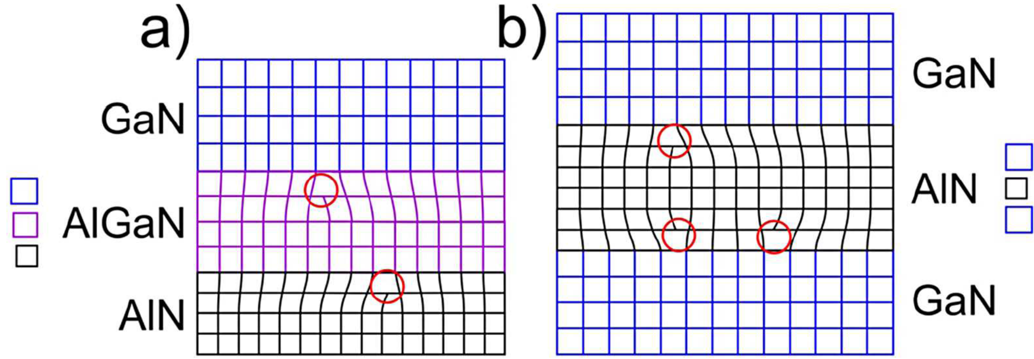


Figure 18: Two different approaches for strain management: graded AlGaN buffer layer (left) and AlN/GaN superlattice (right). The red circles highlight dislocations in the interfaces. The squares on the edges of the figure depict relaxed lattice constants. [1].

The graded AlGaN buffer structure depicted in figure 18a is a common strategy to match AlN and GaN lattices while on the other hand protect the Si surface from gallium. In this approach, the layer composition is graded from AlN to GaN with at least one $Al_xGa_{1-x}N$ layer. Advancing from the AlN layer, each subsequent layer composition is closer to GaN. In addition, the aim is to have the topmost GaN layer under compressive strain although there is some relaxation between the adjacent layers towards the unstrained lattice constant. This interplay is delicate, typically relaxation generates defects in the interface. However, the layer interfaces can bend threading dislocations and, thus, prevent them from advancing to device layers. In figure 18, the dislocations are highlighted with the red circles. The composition grading can be done either in steps or continuously. Step graded buffers can be easier to characterize. On the other hand, continuously graded buffers can lead to higher material quality.

Figure 18b presents a buffer structure that is based on GaN/AlN superlattices. In this approach, GaN is overgrown on partially relaxed AlN layer. The AlN interlayer provides some compressive strain for the overgrown GaN. Some relaxation occurs in the lower GaN/AlN interface but in the upper AlN/GaN interface the amount of relaxation should be reduced. In principle, multiple interlayers can be introduced. However, the accumulating total strain and increasing growth time reduce the usefulness of superlattices.

Plastic deformation of the silicon substrate ultimately limits the amount of possible pre-straining of the epitaxial layers and thus GaN thickness [5]. The III-N materials are resistant for slip plane formation. Indeed, the typical process for tensile stress relief is cracking. However, the plastic deformation of silicon is possible if sufficient strain is generated to the silicon/buffer interface. Silicon becomes relatively soft at high temperatures ($>$1000 °C) associated with MOVPE growth of GaN and AlN [13]. There are few methods for substrate hardening. Increasing the substrate thickness inhibits slip plane formation [5]. In addition, different impurity concentrations are known to increase silicon stiffness [5]. However, typically

the quality is lower for substrates with high impurity concentrations. Moreover, non-standard substrates can be expensive.

Silicon on insulator -substrates have been proposed for substrate hardening [45]. However, it seems that the improvement in strain resistance is overshadowed by increased cost. Strain absorbing layers can lower the substrate stress and provide a more cost effective approach. One approach is to nitridate the silicon surface prior to AlN growth [46]. The strain absorbing silicon nitride allows to grow thicker layers with slightly lower quality [46, 47]. It has been suggested that both AlN and SiN_x can form a coincidence site lattice with the silicon surface [5, 46, 48]. However, the actual interface structure is considerably complex [5, 23, 46, 48].

6.4 Crystal quality

The lattice mismatch between GaN and Si causes dislocations in the film interfaces that advance into the epitaxial layers. The dislocations act as non-radiative recombination routes in optoelectronic devices, lowering the efficiency. In microelectronic applications, the dislocations cause leakage current and lower the breakdown field of the device. Luckily, III-nitride LED light emission is somewhat insensitive to dislocation density compared to other III-V semiconductors [5, 23].

In situ deposited interlayers can be used mimic to the ELOG process. The interlayer approach can be made more cost effective as processing before epitaxial growth is not required. SiN_x interlayers have been applied for dislocation reduction [5, 13, 23]. After certain GaN thickness, a SiN_x layer is deposited. The thin SiN_x layer has some open areas where GaN is exposed and regrowth starts. Threading dislocations in the masked part of the lower GaN layer do not advance to the upper layer. In addition, as the growth starts as faceted GaN islands, some dislocations can bend to in plane and annihilate with other dislocations [23]. The thicker regrown layer it takes for the islands to coalescence the more pronounced this behaviour is. In principle multiple interlayers could be inserted. However, the wafer bow and the achievable crack free GaN thickness place limit on the dislocation reduction.

7 Results

Layers of c-plane GaN were grown on (111) oriented 6" silicon substrates. The film stack consist of AlN nucleation layer, step graded AlGaN buffer and two GaN layers. LED or HEMT active layers could be then grown on the film stack. In this study, the buffer layer scheme is optimized for thin active layers such as those used in HEMTs.

In this chapter the optimization of the temperature profile in addition to the growth process are presented. The growth process was repeated for nine wafers using the same parameters. Although the wafer geometries varied slightly there was no effect on the quality of the grown layers. Next, characterization results of one sample are discussed. The sample was characterized with white light reflection based thickness measurement, wafer geometry measurement and x-ray diffraction. It should be noted that the other samples exhibited similar characteristics.

7.1 Optimizing growth

Temperature calibration of the three zone heater of the MOVPE system founds the basis of other growth optimizing steps. Uniform temperature profile over the whole susceptor surface is vital for achieving similar conditions on the whole wafer surface. Layer composition, thickness, curvature and stresses are effected by the temperature profile. Growth rate is somewhat dependant on temperature, but especially indium incorporation rate is very sensitive to variations. The goal of the calibration is to find set point for the susceptor thermocouple and heater zone balances that result in desired substrate surface temperature.

The calibration process is started by heating the bare susceptor under typical growth conditions albeit without precursor flows. Then the heater zones are balanced to reach radially uniform surface temperature profile at various temperatures. The susceptor is monitored with in situ diode array that provides temperature map based on black body radiation.

After sufficient uniformity is achieved, a substrate is placed on the susceptor. The previous heater zone balancing is then repeated. The substrate somewhat complicates the calibration as the variations are suppressed by increased heat conduction and, on the other hand, the substrate bows according to susceptor surface temperature. Therefore, either the edge or the center of the substrate may become in contact with the susceptor. Finally, a calibration table is created from the various temperature set points and wafer surface temperatures, a piece-wise linear function is fitted to these points.

Fine tuning on the temperature calibration is performed on individual growth processes. This is required as there is an interplay between the film stack structure, curvature and temperature. First, optimization is performed based on the extreme values of the separate monitoring diodes at respective growth steps. Extreme values are used because the measurement is affected by interference of the grown film thickness which typically varies under the diodes. Thus, the values at specific times are not necessarily comparable.

When differences under 5 °C at the different locations on wafer surface are reached, the variations in the diodes prevents further optimizing. Then, the time of the extreme values is employed by interpreting the time differences as differences in film thickness. Elaborate knowledge of the MOVPE growth regime in specific growth step is required in order to link growth rate and temperature (see chapter 3.3). Typically, in GaN growth, the growth regime is mass transport limited growth. Therefore, increasing temperature decreases growth rate as higher temperatures increase the etch rate. In other words, faster growing regions on the wafer have lower temperature.

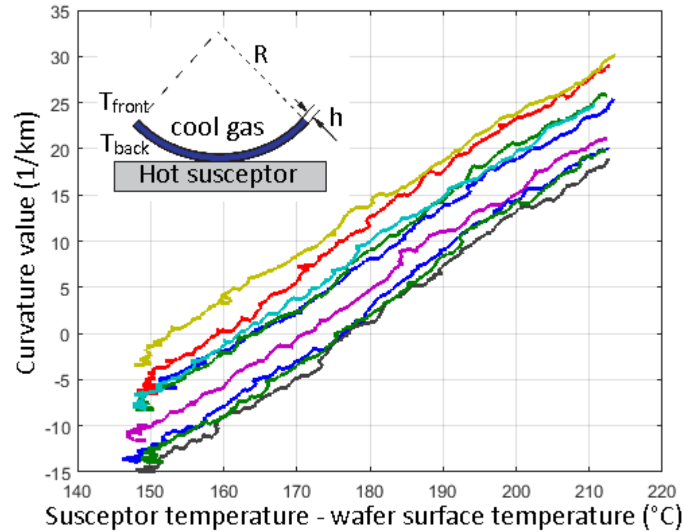


Figure 19: Graph showing curvature values for different wafers as a function of temperature difference between the susceptor and the wafer surface during heating. The inset [35] shows the model used to assess the wafer curvature change.

Vertical temperature difference of the substrate can be estimated using the following method. If the substrate is modelled as a two circle segments separated by the thickness of the substrate (inset of figure 19), a simple relation between the substrate curvature and temperature difference can be formulated

$$\frac{1}{R} = \alpha \frac{T_{back} - T_{front}}{h}, \tag{19}$$

where R, α, T_{back}, T_{front} and h are the curvature, thermal expansion coefficient, front temperature, back temperature and thickness of the substrate, respectively.

Unfortunately, there is no direct way to measure the back temperature of the substrate. The reactor provides thermocouple reading of the susceptor and substrate surface temperature estimated based on blackbody radiation. It was discovered that the substrate curvature in the heating step has a linear relation to the difference of the thermocouple and substrate surface temperature readings (figure 19). Therefore, if we assume that the substrate temperature profile is radially uniform and vertically

linear and use the literacy value for thermal expansion, we can estimate the vertical temperature difference. The radial temperature variation of the substrate during heating was low, 5 °C. Based on figure 19 we can fit a thermal curvature coefficient

$$\frac{1}{R}(T_{thermocouple} - T_{front}) \approx 0.5279 \, \frac{1}{K \ km} \ . \tag{20}$$

Now if we assume a linear dependence between temperature difference of the substrate sides and the temperature difference of the thermocouple and substrate the surface

$$C(T_{thermocouple} - T_{front}) = (T_{back} - T_{front}) \tag{21}$$

we get

$$\frac{1}{R} = \alpha \frac{C(T_{thermocouple} - T_{front})}{h} \tag{22}$$

and finally

$$C = \frac{1}{R}(T_{thermocouple} - T_{front}) \frac{h}{\alpha} \approx 0.12 \ . \tag{23}$$

The linear model presented here has a better agreement with data than a model based on only the substrate surface temperature in reference 35. However, the model in reference 35 was applied successfully for a 2-inch wafer. In addition, the maximum vertical temperature difference was estimated to be under 2 °C [35], for larger and thicker wafers the temperature difference is greater. Based on equation 23 we can estimate the vertical temperature difference over the wafer in GaN growth at 1060 °C to be approximately 24 °C. This result can be used to assess the thermal stresses induced on the silicon substrate during growth. In addition, growth-related wafer bow can be better separated from the thermal bow.

7.2 Growth process

The substrates for GaN growth were 6-inch nominally exact (111) silicon wafers. Thimethylaluminium (TMAl), thimethylgallium (TMGa) and ammonia (NH_3) were used as precursors for aluminium, gallium and nitrogen, respectively. Dopants available were disilane (Si_2H_6) and bis-cyclopentadienyl magnesium (Cp_2Mg) for n-type and p-type GaN, respectively. Hydrogen was used as the carrier gas.

Table 3: Growth parameters for GaN on Si.

Layer	LT-AlN	HT-AlN	$Al_{80}G_{20}N$	$Al_{50}G_{50}N$	$Al_{20}G_{80}N$	GaN 1	GaN 2
Temperature (°C)	980	1085	1060	1060	1060	1040	1040
III/V ratio	336	336	1029	1142	1222	1771	1771
Pressure (mbar)	100	100	100	100	100	100	400
Thickness (nm)	-	255	266	285	468	645	235

Figure 20 presents an example of the wafer curvature, reflectivity at 633 nm and emissivity corrected surface temperature provided by the EpiTT in situ measurement

system. The growth parameters of the layers are presented in table 3. The growth process was started with in situ annealing in order to remove the surface native oxide on the silicon wafer (figure 20a). The annealing was a two step process starting with hydrogen ambient. Then, disilane (Si_2H_6) flow was used to passivate the bare silicon. This is done to prevent roughening of the substrate surface.

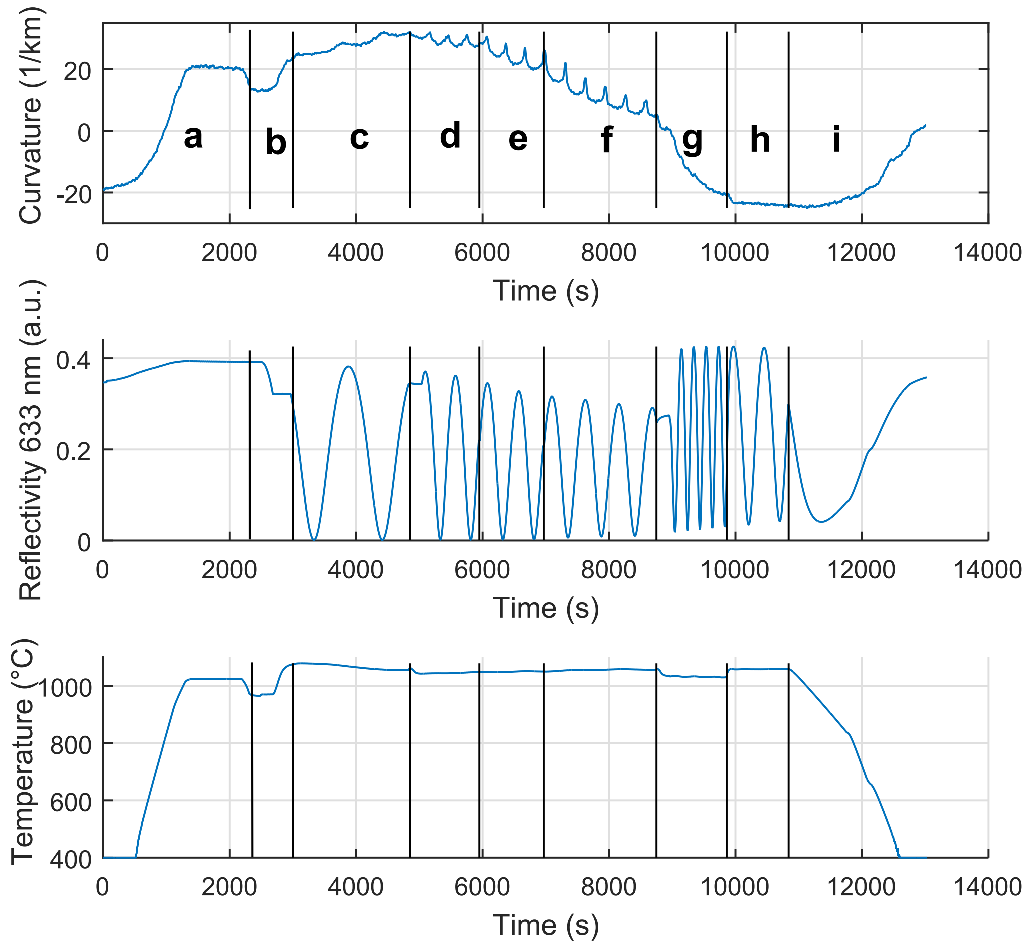


Figure 20: In situ data of GaN on Si growth with process steps: wafer curvature (top), reflectivity at 633 nm (middle) and surface temperature (bottom). The process phases are a) heating and annealing of the substrate, b) low temperature AlN, c) high temperature AlN, d) $Al_{80}G_{20}N$, e) $Al_{50}G_{50}N$, f) $Al_{20}G_{80}N$, g) GaN1 and h) GaN2 layer growth and i) cooling to room temperature. Positive (negative) wafer curvature value is concave (convex).

Low temperature AlN seed layer was used to initiate the growth (figure 20b). Few seconds of ammonia flow was used to nitridate the wafer surface before TMAl flow was started. In this case, the very surface of the wafer is converted to silicon nitride (SiN_x). The silicon nitride acts as a strain absorbing layer [46]. Other alternative

would be to predeposit some aluminium before opening the ammonia line [49]. Al predeposition can be used to increase the quality of the AlN seed layer at the expense of increasing the strain in the epitaxial layers [47]. It has been suggested that SiN_x and AlN can form a coincidence lattice with (111) Si [48]. High temperature AlN was then deposited (figure 20c). The two step growth of the AlN layer increases the buffer quality. It can be seen from figure 20c that the wafer becomes concavely bowed during AlN growth. This indicates that the layer is under tension during this step [13].

After the AlN seed layer, a graded AlGaN buffer was grown. The buffer consisted of three layers with nominal compositions of $Al_{80}G_{20}N$, $Al_{50}G_{50}N$ and $Al_{20}G_{80}N$ (figure 20 d,e and f). The purpose of the buffer is to pseudomorphically match the GaN lattice to the AlN seed layer. However, the large lattice mismatch causes relaxation and defects. The buffer layer induces compressive strain to counteract the thermal stresses induced when the wafer is cooled to room temperature after the growth. It can be seen from figure 20 d,e and f that the concave wafer bow decreases during AlGaN growth. This indicates compressive stress in the film [13].

Finally two layers of GaN were grown with pressures of 100 mbar and 400 mbar for the first and the second layer, respectively (figure 20g and h). The higher pressure increases the quality of the GaN layer. On the other hand, the growth rate is lower. Some dislocation annihilation should occur in the lower layer during growth. Then, device layers would be grown on top of the second thinner layer. As with the AlGaN buffer growth, the GaN layer is grown under compressive strain [13] with increasing convex bow (figure 20 g and h). It can be seen that tensile strain is generated during cooling to room temperature (20i) as the wafer convex bow decreases. This is caused by the thermal expansion mismatch between the epitaxial layers and the silicon substrate.

7.3 Layer thickness

Figure 21 presents the epitaxial layers thickness measurement results. The layer thickness was measured with FilmTek 2000M spectrophotometer. In these results, 10 mm edge exclusion was used because the measured thickness increases substantially on the wafer edge. The wafer thickness map is presented in figure 21a. The wafer flat is towards the bottom of the page. Thickness histogram and statistics are presented in figure 21b. The average thickness of the epitaxial layers was 2.05 μm. The thickness uniformity was good, the standard deviation was 1.1 %. Similar uniformity has been reported for this reactor type [13].

The histogram shows that the thickness mostly follows the normal distribution. However, it can be seen that the distribution has a tail of higher thickness values. This is caused by the non-uniform thickness on the wafer edge which is highlighted in the radial dependency. The radial thickness dependency was studied by integrating the thickness map at certain radius values (21c). It can be seen that the thickness increases when the radius is greater than 60 mm from the wafer center. This behaviour is more prominent if edge exclusion is not used. The thickness values close to the wafer edge are as high as 3 μm. Typically, the growth conditions on the

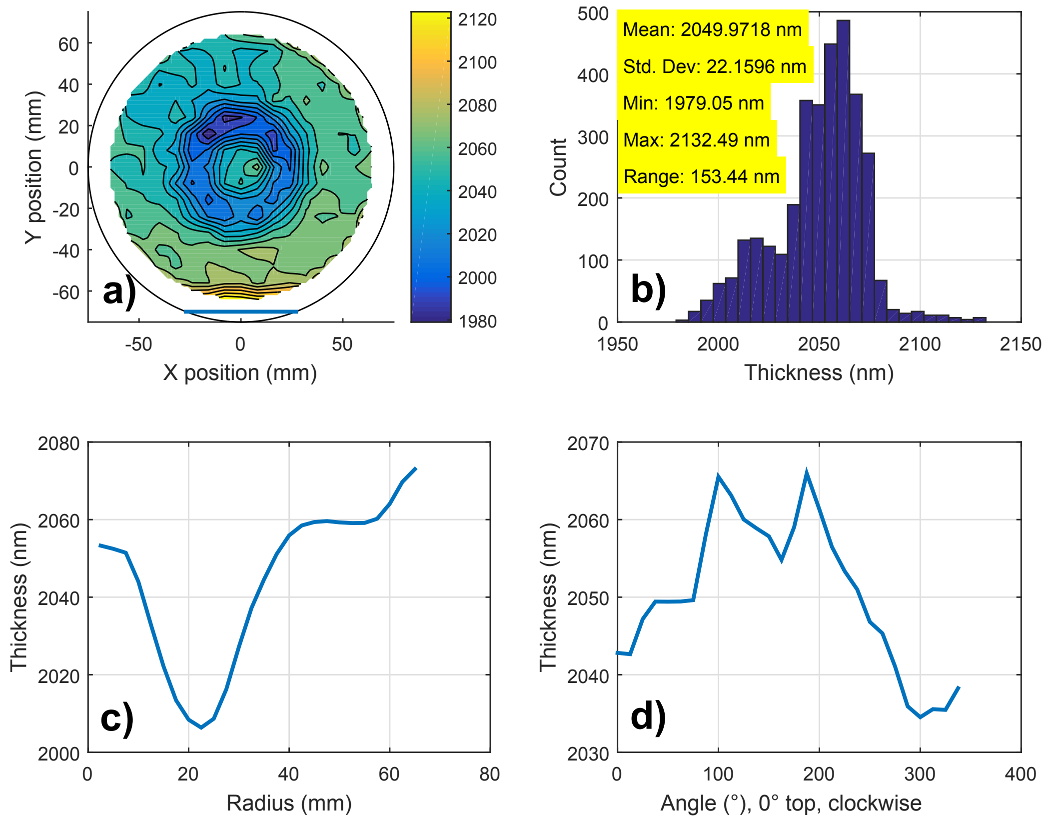


Figure 21: Epitaxial layers a) thickness map, b) histogram, c) radial dependency and d) angular dependency. The edge exclusion of 10 mm was used in this figure.

wafer edge differ from the center. The susceptor pocket edge together with the wafer edge can disrupt the gas flow. Moreover, if the wafer is convex during growth, the wafer edge becomes hotter than the center. Therefore, in the typical mass transport limited growth regime (see chapter 3.3) the growth rate is increased.

It can be seen from the thickness map and the radial dependency that there is a lower thickness area approximately around 20 mm radius (figures 21 a and c). This behaviour has been somewhat mitigated by temperature calibration. However, the area in question is between the two center heater zones (see figure 12). Therefore, the efficient temperature adjustment of this area is challenging. Moreover, the wafer curvature evolution during growth further complicates this issue. The ARGUS based temperature optimizing (see chapter 7.1) suggests that most of this thickness non-uniformity is created during the final GaN growth step. Therefore, further growth optimizing should be directed for this process step.

Figure 21d presents the angular thickness dependency. The angular thickness dependency was studied by integrating the thickness map at certain angle values. The zero angle is at the wafer top and the angle increases clockwise. It can be seen that the thickness increases at the wafer flat, close to 180°. This is caused by the

wafer edge disturbance to the gas flow and to the temperature profile. It could be beneficial to limit this non-uniform area for example by using a dummy silicon piece. Indeed, in larger wafers, manufactures are using a smaller feature called a notch to mark the wafer orientation.

There seems to be another angular thickness dependency in addition to the wafer flat induced thickness non-uniformity. It can be seen that the epitaxial layer has a higher thickness at lower angle values, below 180°. In addition, the thickness variance is not symmetric with respect to the wafer flat. This might suggest that the susceptor is not perfectly symmetric. Similar behaviour was observed on other growth runs. Showerhead and heater coil angular dependencies should be minimal because the wafer is rotated. However the wafer is fixed to the susceptor. It might be beneficial to place the wafer so that the effects of the flat and the susceptor limit each other.

7.4 Wafer geometry

The wafer profile was measured with a KLA Tencor Ultra Gage 9500 system. Figure 22 presents the wafer height profile map and surface height curve before the epitaxial layer growth. It can be seen that the wafer is relatively flat. The three point bow of the wafer is 7.4 μm. In other words, the curvature of radius is 380 m. Bow under 10 μm is typical for 6-inch wafers. The silicon ingot processing creates some variance in the wafer geometry.

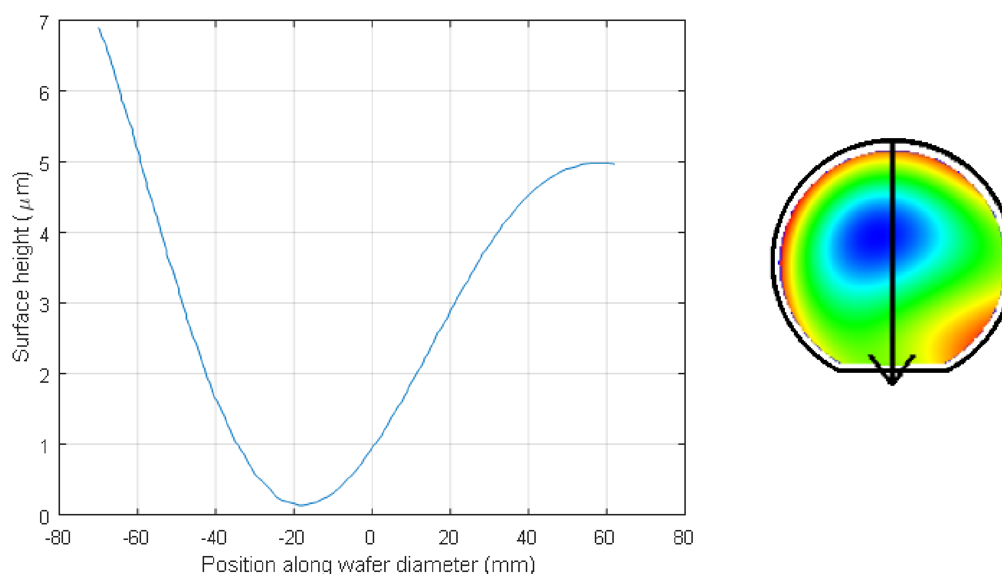


Figure 22: Wafer height profile before epitaxial growth: a line scan (left) and a wafer map (right). The arrow on the wafer map depicts the scan direction.

Figure 22 presents the wafer height profile map and surface height curve after the epitaxial layer growth. It can be seen that the wafer has become clearly more concave. This is caused by the mismatch in the thermal expansion coefficients of

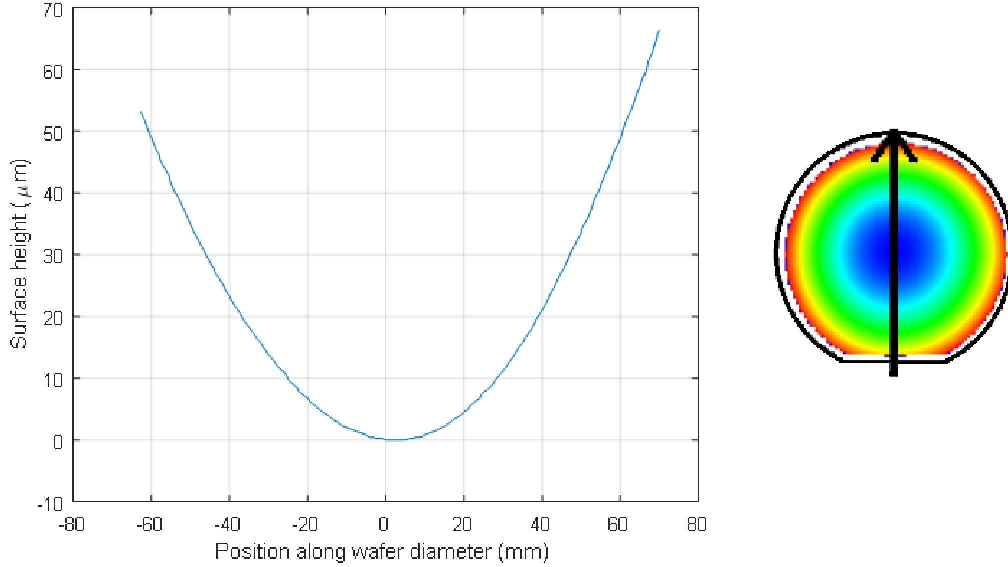


Figure 23: Wafer height profile after epitaxial growth: a line scan (left) and a wafer map (right). The arrow on the wafer map depicts the scan direction.

silicon and grown III-N layers. The bowing is also non-spherical, most likely caused by the thickness non-uniformity. The three point bow of the wafer was 80.1 μm. The curvature of radius was 34.7 m. Surface height for post processing should be under 50 μm [13]. The 80.1 μm bow value is on the upper limit for processing. However, the growth process with the same parameters has yielded several wafers within this specification. On the other hand, all of these wafers have been concavely bowed. The buffer layer could be made thicker or use more Al containing alloys to pre-stress the GaN layers. This should result in less bowed wafers after cooling to room temperature.

7.5 X-ray diffraction

Two reciprocal space measurements were conducted for the epitaxial layers. Figure 24 presents the symmetric (002) and the asymmetric (105) reciprocal space maps (RSM). In both maps, the peaks from top to bottom are created by layers: AlN, $Al_{80}G_{20}N$, $Al_{50}G_{50}N$, $Al_{20}G_{80}N$ and GaN. The peak intensity is decreasing as the layer distance from sample surface increases. The x-rays are attenuated by sample scattering.

Using these measurements together with equations 14 and 15 the lattice constants of the GaN layer can be calculated. For the lattice constant c we get

$$c = \frac{\lambda}{sin(\theta_{002})}, \tag{24}$$

where θ_{002} is the theta angle of maximum intensity in the (002) reflection and λ is

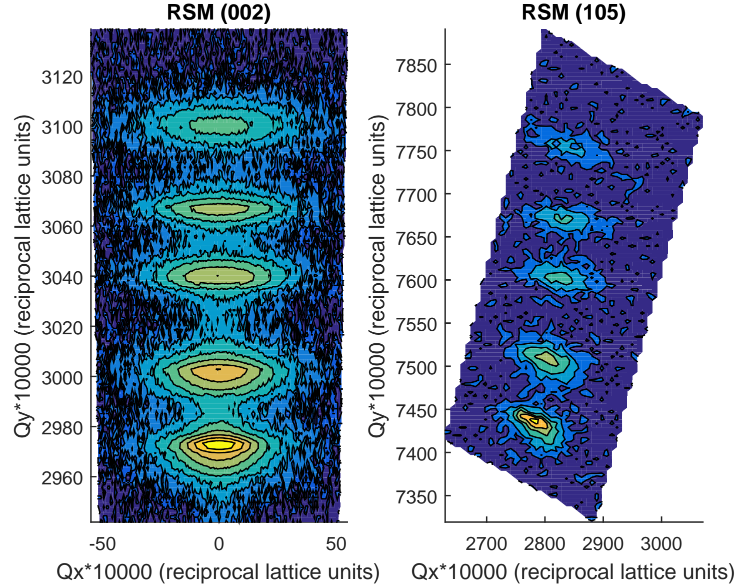


Figure 24: Reciprocal space maps based on XRD measurements: (002) reflection (left) and (105) reflection (right).

the x-ray wavelength. Similarly, for the in plane lattice parameter:

$$a = \frac{2\lambda}{\sqrt{3}\sqrt{4sin(\theta_{105}) - 25sin(\theta_{002})}}, \tag{25}$$

where θ_{105} is the theta angle of maximum intensity in the (105) reflection. The x-ray wavelength $\lambda = 0.1540560\ nm$ for the copper $K\alpha_1$ emission line used in this study [15]. The calculated lattice constants are $a \approx 0.3204$ nm and $c \approx 0.5180$ nm. The reported values for relaxed GaN are $a \approx 0.3189$ nm and $c \approx 5.185$ nm [2]. The grown GaN layer has a slightly larger a lattice constant and, on the other hand, smaller c lattice constant than the relaxed value. Therefore, the GaN layer is under tension at room temperature. This is characteristic for GaN on Si growth.

It can be seen from the (105) scan (figure 24) that the layer peaks are not located at the same Q_x coordinate. This indicates partial relaxation in the interfaces between the layers. Relaxation in the interfaces and the dislocations generated in the process cannot be avoided in this type of an AlGaN system. The lattice mismatches between the materials are too great for perfectly pseudomorphic growth of device thickness GaN layer [1,5]. Instead, some dislocation annihilation techniques should be applied.

The full width at half maximum (FWHM) of the (002) and (105) omega scans were 800 and 770 arcsec, respectively. FWHM values for the (002) omega scan of 220 to 750 arcsec have been reported [12, 50, 51]. The FWHM of the scan can be related to material quality [37, 42]. However, multiple factors can cause the peak broadening [37]. In the case of GaN on Si, typically the material quality dominates [37]. Dislocation density can be roughly estimated from the peak broadening [37]. However, a more accurate method would be to etch the GaN surface and image the resulting dislocation pits with atomic force microscopy [5, 23]. In addition, the

electrical properties could be characterized with Hall measurements [5].

The layer quality of the grown GaN is comparable to the values that have been reported. However, the quality seems to be in the lower range. Nevertheless, the grown GaN layer quality is sufficient for device processing. It should be noted that the grown layer is quite thin and no dislocation annihilation techniques were used. For example, in situ grown SiN_x layers in addition to growing thicker layers have been found to increase material quality [5, 13, 23]. In addition, using Al predeposition, as opposed to nitridation, to initiate the growth should decrease defect density [5, 49].

8 Conclusion

C-plane GaN layers were grown on (111) 6-inch silicon substrates by MOVPE. The surface native oxide was removed by in situ thermal annealing. Step graded AlGaN buffer layer was used to match the lattice of GaN to Si and for strain engineering. The buffer scheme is optimized for a thin active device area such as a HEMT. Low temperature and high temperature AlN were used as the nucleation layer to provide base for the buffer and protect the substrate surface from meltback etching. The two step buffer growth should increase the layer quality. The growth was initiated with ammonia preflow to nitridate the substrate surface before AlN deposition. The nitridation should decrease the strain of subsequent layers [46, 47]. Two GaN layers were grown on the buffer stack. The thicker lower layer should provide some dislocation reduction. The upper layer was grown at a higher pressure to increase the quality. Device layers would be then grown on top of the second layer.

The epitaxial layer thickness was mapped with a spectrophotometer. The total film thickness was approximately 2.05 μm. The thickness uniformity was good, the standard deviation was 1.1 % (10 mm edge exclusion). Similar uniformities have been reported for this reactor type [13]. However, the layer thickness increased as much as 3 μm on the wafer edges. This indicates non-uniform growth conditions. Moreover, there is a consistent thickness non-uniformity on the wafer. In-situ measurements indicate that this is created during the GaN layer growth. In addition, the wafer flat causes some non-uniformity. Finally, it seems that the susceptor has some inherent non-uniformity.

The wafer geometry was studied. The wafer had become concavely bowed after growth. The bow was 80.1 μm. The bow was non-spherical probably due to thickness non-uniformity. Wafer bow under 50 μm would be preferred for device processing for 6-inch wafers [13]. However, the growth process with same parameters has yielded several wafers within this specification.

Resiprocal space maps around (002) and (105) reflections were measured with XRD. The lattice constants of GaN were calculated. The GaN layers were under tensile strain at room temperature, based on the lattice constants. The ω-FWHM of the (002) and (105) scans were 800 and 770 arcsec, respectively. These are the on the upper range of reported values [12, 50, 51]. However, dislocation reduction techniques were not employed for the grown layers. Nevertheless, the grown GaN layer quality is sufficient for device processing.

Following subjects should be further investigated. The radial temperature settings should be calibrated for the GaN growth steps in order to increase layer thickness uniformity. The wafers were concavely bowed at room temperature even without active layers. Therefore, the a thicker buffer possibly with higher Al content should be used. Some dislocation reduction techniques such as SiN_x interlayers should be considered to increase crystal quality [13]. In addition, aluminium predose instead of the nitridation could increase the layer quality [5]. Finally, using hardened substrates the wafer bow could be decreased [5]. For example, substrates with higher impurity concentrations could be studied.

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