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Coatings for ALD Reactors to Prevent Metal Contamination on Semiconductor Products

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M.Sc. Thesis

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The research was done in Beneq Oy

12 / 2019

HELSINGIN YLIOPISTO – HELSINGFORS UNIVERSITET – UNIVERSITY OF HELSINKI

Tiedekunta – Fakultet – Faculty	Koulutusohjelma – Utbildningsprogram – Degree programme
Faculty of Science	Inorganic Materials Chemistry

Tekijä – Författare – Author

Iiris Milja Tuoriniemi

Työn nimi – Arbetets titel – Title

Coatings for ALD Reactors to Prevent Metal Contamination on Semiconductor Products

Työn laji – Arbetets art – Level	Aika – Datum – Month and year	Sivumäärä – Sidoantal – Number of pages
M.Sc. Thesis	12 / 2019	90

Tiivistelmä – Referat – Abstract

Atomic layer deposition (ALD) is a promising processing method for the next generation semiconductor devices. Major advantages of ALD include conformality, uniformity over large areas, precise thickness control, repeatability and high quality of films produced. ALD thin film deposition is done inside an ALD reactor. Typical construction materials of ALD reactors include metal alloys such as stainless steel, aluminum and titanium. These materials contain multiple metallic elements that can be detrimental to the performance, reliability and yield of semiconductor devices.

In order to process semiconductor devices with ALD, metal impurity levels originating from the ALD reactor must be controlled. Allowed levels of metal impurities in semiconductor processing are stringent and showing a tightening trend. This has led into the development of new methods for contamination control together with the adoption of more sensitive and robust detection methods for metallic impurities, such as inductively coupled plasma mass spectrometry (ICP-MS).

This master thesis focuses on the metallic impurities originating from an ALD reactor and their prevention with ALD coatings. Three typical construction materials, aluminum, titanium and stainless steel were examined. The studied coatings were ALD deposited aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and their nanolaminate (Al_2O_3/HfO_2). The ability of the coatings to prevent metal impurity transfer from the metals to silicon substrates through the gas phase was studied by exposing the coated metals to two ALD precursors, trimethyl aluminum (TMA) and tris(dimethylamino) cyclopentadienyl hafnium ($CpHf(NMe_2)_3$). Metal impurity concentrations on silicon were measured with ICP-MS.

Since academic literature concerning control of metal contamination from ALD reactors does not directly exist, the literature part of this thesis was based on relevant related topics. The selected topics included the development of semiconductor industry, role of ALD in this development and new ALD materials and chemistries required. Additionally, protective ALD films and the effects of metal impurities in semiconductor products were reviewed. The overall conclusion of this study was that the ALD coatings provide a worthy solution for metal contamination control. Some differences between the passivation efficiencies of different metal – coating systems were found.

Avainsanat – Nyckelord – Keywords

Metal contamination, Atomic Layer Deposition, ALD, Semiconductors, Integrated Circuits, Thin film, Corrosion

Säilytyspaikka – Förvaringställe – Where deposited

E-thesis

Muita tietoja – Övriga uppgifter – Additional information

This thesis was done in Beneq Oy.

Contents

Abbreviations

AI = artificial intelligence

ALD = atomic layer deposition

BEOL = back end of line

CIGS = $Cu(In,Ga)Se_2$

CVD = chemical vapor deposition

DRAM = dynamic random access memory

egTMA = electronic grade trimethyl aluminum

EOT = equivalent oxide thickness

FEOL = front end of line

FEP = front end process

GDP = gross domestic product

GF-AAS = graphite furnace atomic absorption spectroscopy

GOI = gate oxide integrity

HEMT = high electron mobility transistor

HVM = high volume manufacturing

ICP-MS = inductively coupled plasma mass spectrometry

ICs = integrated circuits

IoT = internet of things

IPA = isopropyl alcohol, isopropanol, 2-propanol

IRDS = International Roadmap for Devices and Systems

ITRS = International Technology Roadmap for Semiconductors

LED = light emitting diode

LOD = limit of detection

MEMS = micro electro mechanical system

MIM = metal-insulator-metal

MOSFET = metal-oxide-semiconductor field effect transistor

MtM = More than Moore

SEM = scanning electron microscope

SIA = Semiconductor Industry Association

SiP = system in package

SoC = system on chip

TFE = thin film encapsulation

TFEL = thin film electroluminescent display

TMA = trimethyl aluminum

TOF-SIMS = time-of-flight secondary ion mass spectrometry

TXRF = total reflection X-ray fluorescence

VPD = vapour phase decomposition

VR = virtual reality

WSTS = World Semiconductor Trade Statistics

XRD = X-ray diffraction

1. Introduction

Demand for new, more powerful, highly functional yet smaller and portable microelectronic devises appears to be never ending. The development of microelectronics industry has long followed Moore's law, the prediction that number of transistors per integrated circuit doubles every second year.[1] However, the continuous downscaling of devises has led into problems that will inevitably hinder the pace of Moore's law and most likely result in saturation of the line of transistor count per chip of each year. Even though Moore's law as such will no longer hold in the future, the development of microelectronics will continue and generate new forms such as More Moore and More than Moore. New generations of integrated circuits have required introduction of new materials together with new deposition methods to the semiconductor industry. One of these promising deposition methods, already in use in semiconductor fabrication, is atomic layer deposition (ALD).

The main advantage of ALD is the conformality of the resulting films. Other advantageous features associated with ALD include precise film thickness control, high quality of the films together with good uniformity and reproducibility.[2,3] All these desirable features originate from the self-limiting surface reactions of the alternately supplied precursors. As the devise structures in the integrated circuits have become more complex and the overall device size has decreased, also the film structures have become thinner and more complexly shaped. Thus, atomic layer deposition appears to be the perfectly matching deposition method for these applications. Even the intrinsic slowness of ALD, usually considered as the main drawback of the method, is compensated as the desired film thicknesses are decreased.

As the devise dimensions together with film thicknesses decrease, the role of contamination control must be highlighted. With thinner films the tolerable contamination concentrations are lower than with thicker ones. The role of contamination is crucial in IC production, since over 50 % of the yield losses in the manufacturing are caused by it.[4] The inevitable need for contamination control has led into the development of more efficient cleaning techniques for silicon wafers as well as to the determination of specifications for the tolerable contamination concentrations. As the tolerable concentrations have decreased and the materials selection has diversified, the need for reliable, high sensitivity, multicomponent analysis methods have risen.

One of the most harmful type of contamination is metal contamination. Metal contamination can originate from multiple sources and it can be detrimental to the semiconductor products in a variety of ways potentially harming the device performance, reliability and yield. Some of the most studied and harmful metallic impurities in semiconductor industry include copper and iron. Heavy metals in general are considered especially detrimental to the device performance but in practice all metals can cause detrimental effects. However, the tolerance to metal impurities in general and for each separate element depends on the application and manufacturing step.

One factor that must be considered when processing ICs with ALD is the purity of the ALD reactor. Reactors are typically constructed from materials including metal alloys such as aluminum, titanium and stainless steel. These materials are possible sources for the metal contamination. Especially when the reactor is exposed to the aggressive precursors used in ALD, the risk for the metal contamination is obvious. The aggressive nature of the ALD precursors guarantees the saturation of the surface reactions in a short time.[5] With milder reactants many good features of ALD would be sacrificed. Additionally, ALD is in most cases carried out at elevated temperatures, typically in the range of 70–500 °C. Heating increases diffusion and transportation of metal species. Thus, methods to protect the components being processed from the metal contamination originating from the ALD reactor are needed.

Academic literature addressing directly the problem of the metal contamination originating from thin film processing reactors does not exist. However, patents related to corrosion protection of processing equipment,[6,7] prevention of flaking off of the film from chamber walls[8,9] and reduction of metal contamination originating from the processing reactor[10] can be found. All these patents rely on film deposition or enhanced native oxide formation on the metal surface.

Corrosion protection of metal surfaces with ALD films is a well-studied but versatile topic also in the academic literature. Corrosion preventing films include primarily oxides, especially Al_2O_3 but other oxides such as TiO_2, Ta_2O_5, SiO_2, HfO_2 and ZrO_2 have been studied as well.[11] Another, corrosion related application of ALD are diffusion barriers for metals as an example in interconnects of ICs. These barriers include mostly metal nitride films.[11] All in all, ALD coatings appear to provide a viable method for isolating the metal surface from the surrounding environment.

The focus of this thesis is on the role and future possibilities of ALD in semiconductor industry. Emphasis was placed on metal contamination, its effects and ways to prevent it in the ALD processing step. The motivation for this project was the increasing demand for conformal, well controllable and high-quality thin film deposition methods in the semiconductor industry. In the experimental part, a proposition to solve the problem of metal contamination originating from the ALD reactor by depositing thin oxide films by ALD is given and its viability is tested. Contamination analysis were carried out with ICP-MS covering 36 metallic elements. The literature part of this thesis reviews the general development and trends in semiconductor industry, ALD deposited films in semiconductor devises, effects of metal contamination in these devises, analysis methods for metallic impurities and the use of protective ALD films against corrosion and diffusion.

LITERATURE REVIEW

2. Semiconductor industry

2.1 Introduction to semiconductor industry

Semiconductor devices, also known as semiconductor components, include e.g. transistors, capacitors, resistors and diodes. A common factor to these devices is that they are made of semiconductor materials – materials whose conductivity is between an insulator and a conductor. This originates from the band structure of semiconductors, in which the bandgap is between that of an insulator and a conductor (Figure 1). The most common substrate material for semiconductor devices is silicon (Si), but compound semiconductors such as gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (InP), indium gallium arsenide (InGaAs), silicon carbide (SiC) and gallium antimonide (GaSb) are also used.

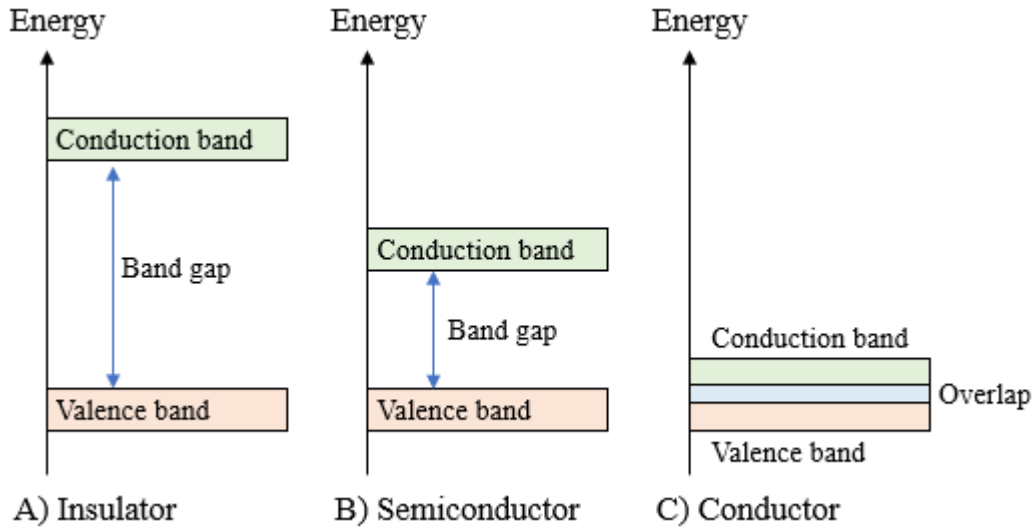

Figure 1. Illustration of the differences in band gaps between insulators, semiconductors and conductors.

One special feature of semiconductors is the possibility of affecting the electrical properties by doping. By introducing selected "impurities" i.e. foreign atoms with a certain number of valence electrons to the semiconductor, the conductivity of the material can be tuned, thus creating n- and p-type semiconductors (Figure 2). As an example, silicon has four valence electrons and it can be doped with elements that have one more or one less valence electron. If a group 15 element is introduced into the silicon lattice, the extra electrons originating from the dopant act as negative charge carriers thus creating an n-type semiconductor. Similarly, when the dopant is from the group 13, the lack of the fourth valence electron

creates holes, which act as positive charge carriers thus creating a p-type semiconductor. These unique features of conductivity are utilized in semiconductor devices.

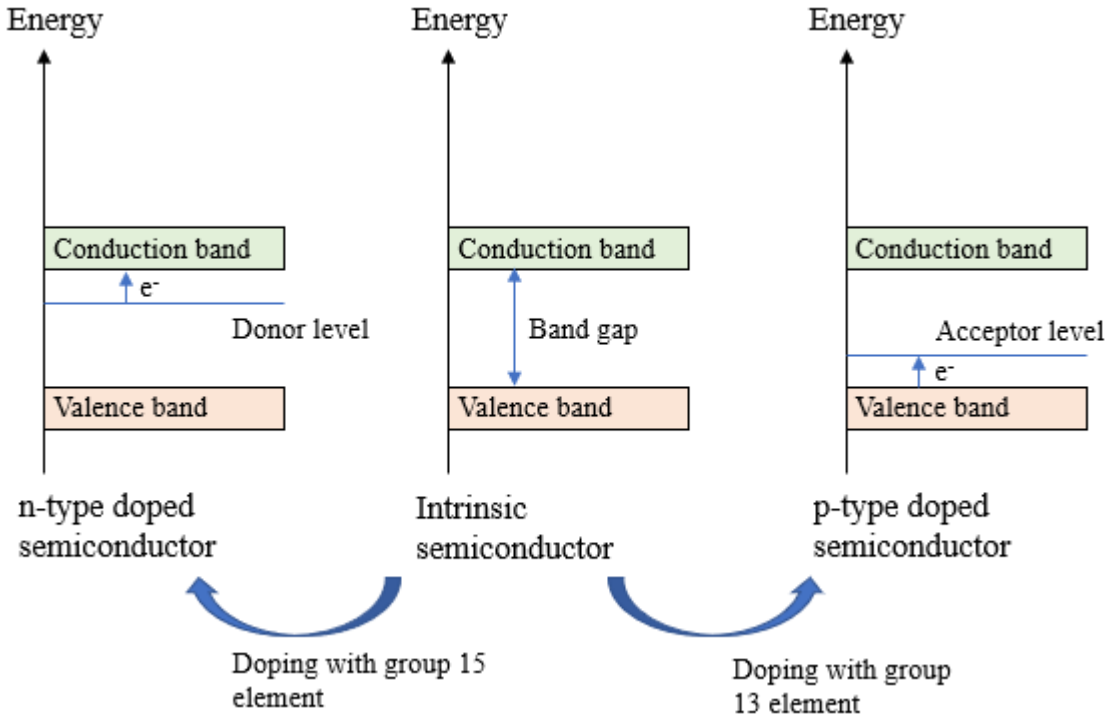

Figure 2. Doping of semiconductor materials by introduction of foreign atoms.

Applications of semiconductor devices are versatile. Semiconductor devices play a key role in modern electronics in communications, computing, health care, defence, transportation and clean energy production, but they are also used in emerging technologies such as artificial intelligence (AI), virtual reality (VR) and internet of things (IoT) (Figure 3).[12] According to Semiconductor Industry Association (SIA) the annual global sales of semiconductors was 412 billion U.S. dollars in 2017.[13,14] The sales show a growing trend according to SIA and the World Semiconductor Trade Statistics (WSTS).[13,14]

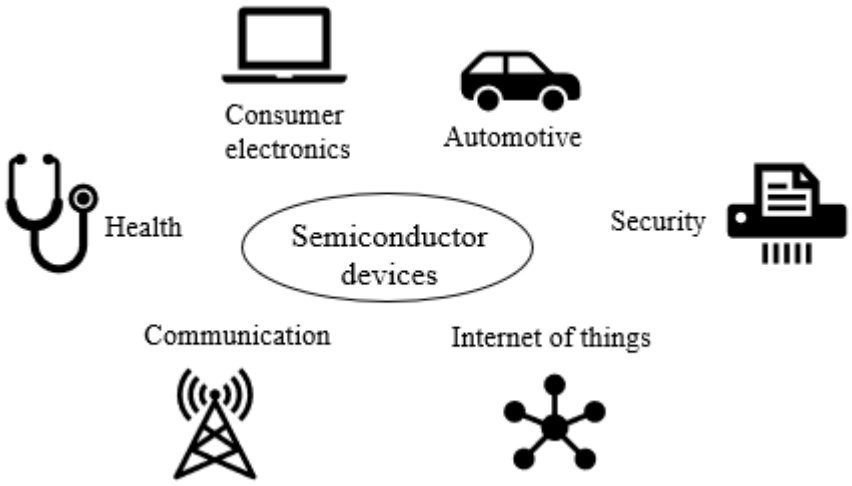

Figure 3. Examples of application areas of semiconductor devices.

One of the most important application of semiconductors is integrated circuits (ICs, microchips, chips, dies). Integrated circuits are clusters of interconnected components, including transistors, that are built on a semiconductor surface, traditionally on silicon. ICs are manufactured on silicon wafers so that one wafer consists of hundreds to thousands of ICs, depending on the sizes of the ICs and the wafer. Each of these ICs or "chips" can contain up to several billions of transistors (Figure 4). In the IC manufacturing process steps related to the wafer processing are called front end processes (FEP) or front end of the line (FEOL) processes, and process steps related to chip packaging i.e. assembling the chips into the packages where they are used are called back end of the line (BEOL) processes. One key measure of the progress of semiconductor industry has been the number of components that can be fitted into a single chip. The increase in the number of components per chip has been extremely fast, which was predicted already in the 1960s by Gordon Moore – the constructer of Moore's law.

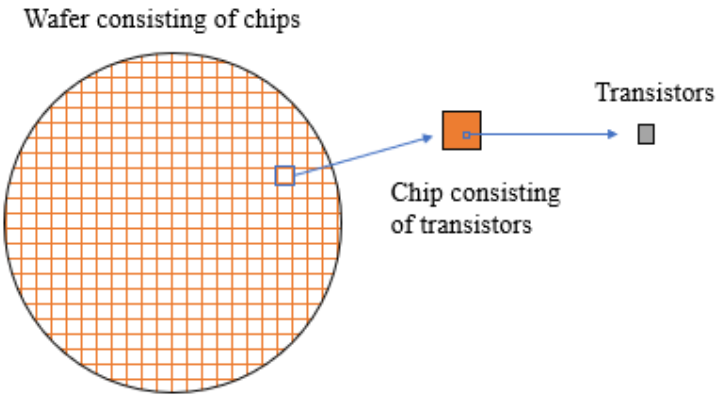

Figure 4. Schematic illustration of a wafer containing integrated circuits with transistors. The wafer can contain hundreds of chips, each of which can contain up to several billions of transistors.

2.2 Moore's law

A driving factor in the development of integrated circuits has been Moore's law, a prediction that the number of components per integrated circuit doubles every year. This prediction was made by Gordon Moore in 1965 and was updated by him a decade later to state that the number of components doubles only every second year.[1] Although this law is not a natural one, but merely economical – the urge to meet the Moore's law has been an effective driver for the IC development and has led into the evolution of new generations of integrated circuits and microelectronics. The transistor count as a function of the year of introduction is illustrated in Figure 5.

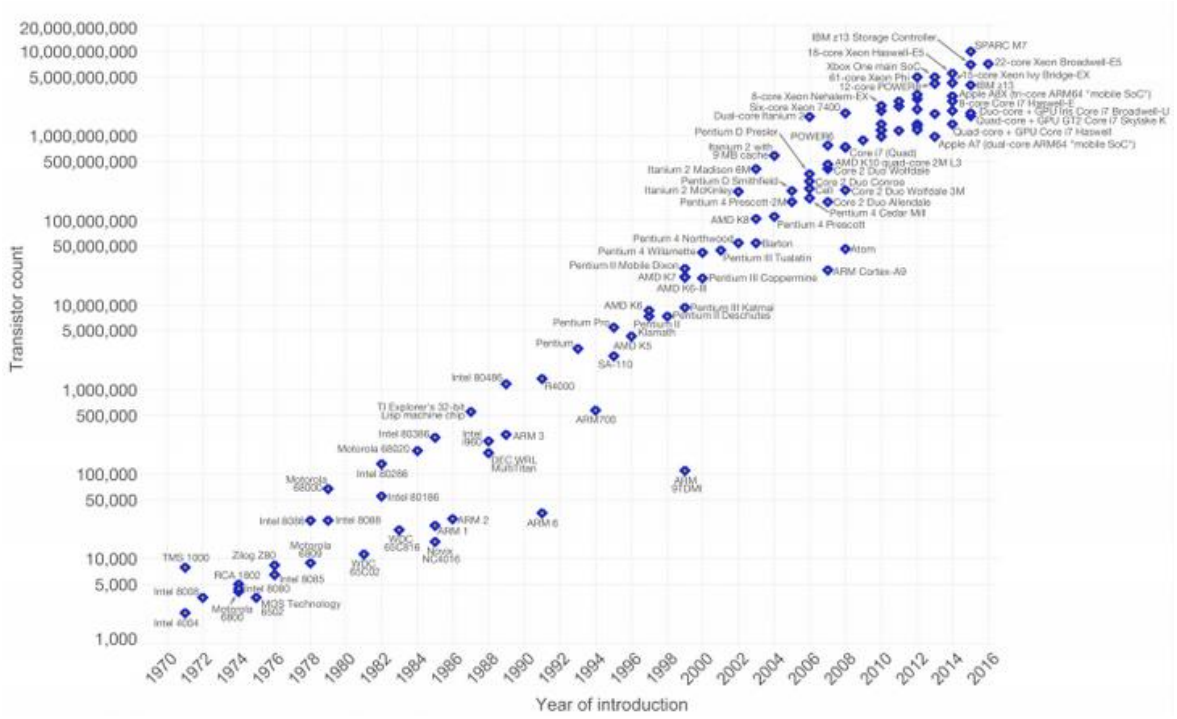

Figure 5. Number of transistors per chip (logarithmic scale) as a function of the year of introduction.[15] Doubling of transistor count every other year supports the Moore's law. Data visualization from OurWorldinData.org licensed under Creative Commons BY-SA.

In the beginning of this development, the focus was in downscaling of feature sizes. As the feature sizes got smaller, ICs became more efficient and consumed less power. Also, more transistors could be fitted into each chip. However, eventually the continuous shrinking of the components started to cause problems. The first negative effect of the downscaling was excessive heat generation in the chips. This was compensated by limiting the speed of electrons in the circuits and by re-designing the structures to maintain and improve their efficiency. However, with further downscaling another problem occurred. With thin enough material layers quantum effects started to take place, causing for example leakage currents.[16]

To overcome the challenges that were faced due to the component size shrinking, new materials, re-designed device structures and new processing technologies were needed in the IC manufacturing.[16,17] This required constant introduction of new innovations and more sophisticated fabrication tools and processes into the field. The development of integrated circuits can be divided into different eras in which different methods have been used to ensure the continuity of Moore's law. Table 1 describes the eras of IC development as the International Roadmap for Devices and Systems (IRDS) presented them in 2017.[18] IC technology generations have also been described as technology "nodes", where a smaller

node means more advanced generation, as an example one may refer to “90 nm”, “22 nm” or “10 nm” technology nodes. Originally the technology nodes were named after the physical dimensions of DRAM devices. This is however not the case today as the term node is used with other types of ICs than DRAMs as well, and the node does not stand for any specific physical dimension but is merely a number.

Table 1. Ages of scaling of semiconductor components in ICs.[18]

Age of scaling	**Era**	**Explanation**
Geometrical scaling	1975–2002	Reduction of horizontal and vertical dimensions in planar transistors.
Equivalent scaling	2003–2024	Reduction of only horizontal dimension, application of new materials, vertical structures replace planar transistors.
3D power scaling	2025–2040	Transition to completely vertical device structures.

Two fundamental factors of Moore’s law are capability and cost.[19] The component performance has been increasing with the component development but the price per area has been increasing due to the requirement of more sophisticated processing techniques. However, the key factor, cost per transistor, is affected by both cost per area and area per transistor (Equation 1).[19] The increase in cost per area has been compensated by the decrease in transistor area, which has made the reduction in cost per transistor possible. Mass production of integrated circuits, yield enhancement as well as increasing wafer sizes have been essential contributors to this price development as well.[20] Low enough transistor prize is essential in keeping the components viable in electronics and thus available to common consumers.

$$\frac{\text{cost}}{\text{transistor}} = \frac{\text{cost}}{\text{area}} \cdot \frac{\text{area}}{\text{transistor}} \qquad (1)$$

2.3 Second life of Moore’s law – More Moore and More than Moore

As the IC market has reached the scale beyond which further downscaling is not straightforward, does not guarantee better device performance and might not be economically viable, new perspectives to Moore’s law have risen: “More Moore” and “Moore than Moore” (MtM).[21] More Moore is the conventional approach for further downscaling of components, applicable for digital memory and logic technologies.

Downscaling of the components is done considering all the key parameters: performance, power, area and cost.[22] The other approach, More than Moore, concentrates on applying non-digital technologies such as radiofrequency communication, sensors, actuators and biochips into the integrated systems. These components are based on silicon technology but do not follow the Moore's law. Figure 6 presents the relationship between More Moore and More than Moore in integrated systems as Arden et al. presented it in their "More-than-Moore" White Paper.[23]

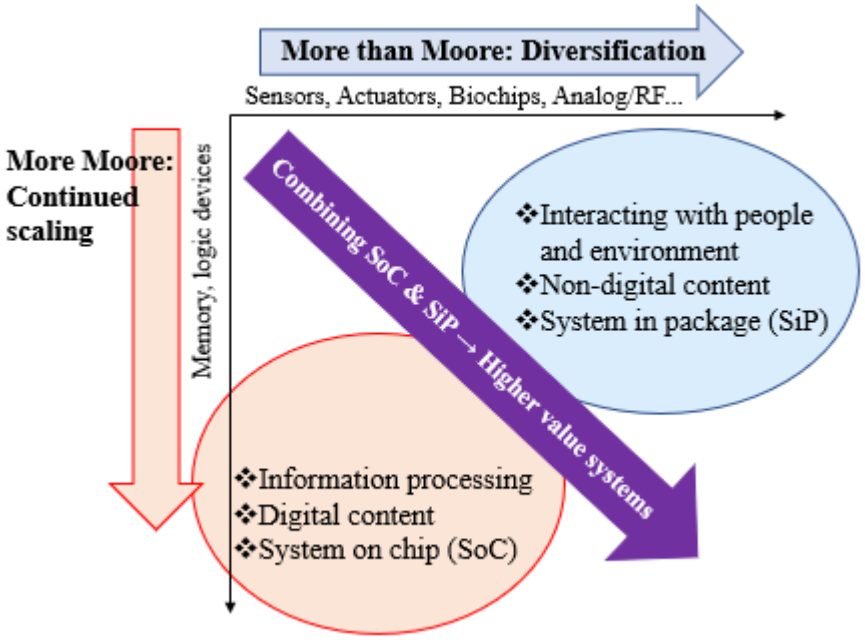

Figure 6. More Moore and More than Moore in the development of integrated systems according to Arden et al.[23]

The aim of the conventional More Moore miniaturization is to provide efficient devices for information processing. The aim of the More than Moore perspective is to add diversity and functionality making the interaction between the electronic devices and their surroundings and users possible. The most powerful prospect for this development is to combine the digital and non-digital functionalities in compact systems, either in a system on chip (SoC) or a system in package (SiP). This heterogeneous integration is the way of producing new, more efficient and functional microelectronic products. Another difference between the More Moore and More than Moore developments is that More Moore, originating from the Moore's law has been technology driven but the More than Moore development has been driven by applications. Comparison of More Moore and More than Moore is presented in Table 2.

Table 2. Comparison of factors in More Moore and More than Moore.[23]

Factor	**More Moore**	**More than Moore**
Content	Digital	Non-digital
Driver	Technology	Applications
Benefit	Downscaling	Diversification
Design	SoC	SiP
Function	Information processing, computing	Interaction with people and surroundings
Device examples	Memory and logic, CMOS	RF, sensors, biochips etc.

Heterogeneous integration, more viable microelectronic products

3. ALD in semiconductor industry

3.1 Principle of ALD

Atomic layer deposition is a gas phase thin film deposition method resembling chemical vapour deposition (CVD). The main difference is that in ALD precursors do not meet in the gas phase but are introduced into the reaction chamber sequentially. Between the precursor pulses the chamber is purged with an inert gas to remove the excess precursor and gaseous by-products. Thus, a typical ALD cycle consists of four steps: 1) pulse of the first precursor, 2) purge, 3) pulse of the second precursor and 4) purge. An example of an ALD cycle is presented in Figure 7.

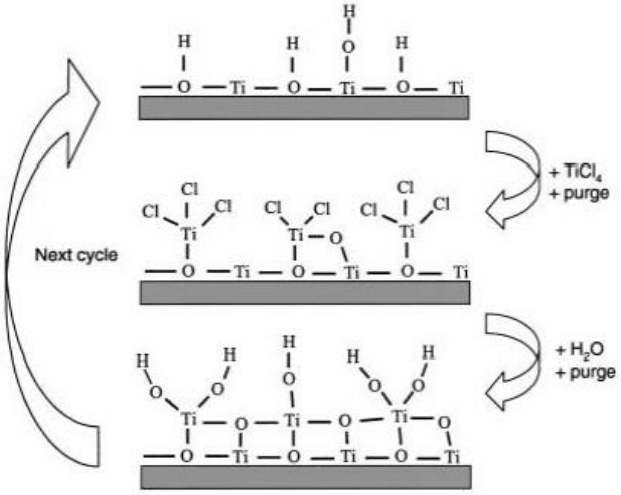

Figure 7. Schematic presentation of an ALD cycle with H_2O and $TiCl_4$ precursors to deposit TiO_2.[2] Reprinted with permission from M. Leskelä and M. Ritala, *Angewandte Chemie International Edition*, 2003, **42**, 5548–5554. Copyright 2003 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Ideal ALD growth is saturative, which means that only a certain amount of the precursor will react with or be chemisorbed onto the substrate surface after which no more precursor will be consumed (Figure 8A).[2,3] This ideal growth can be violated if precursor decomposition or etching reactions are involved in the growth (Figure 8A). Saturation of the surface reactions makes the film growth self-limiting (self-terminating), which means that the amount of material deposited in each cycle is constant. Thus, the film thickness can be precisely controlled by applying a chosen number of cycles (Figure 8B). Besides the thickness control, several other advantages follow from the self-limiting growth, including conformality, uniformity, precise composition control and reproducibility.[2,3] The ability to deposit films uniformly with precise thickness control is demonstrated in Figure 9A which

shows a nanolaminate structure. Conformality of an ALD film in a trench structure is demonstrated in Figure 9B.

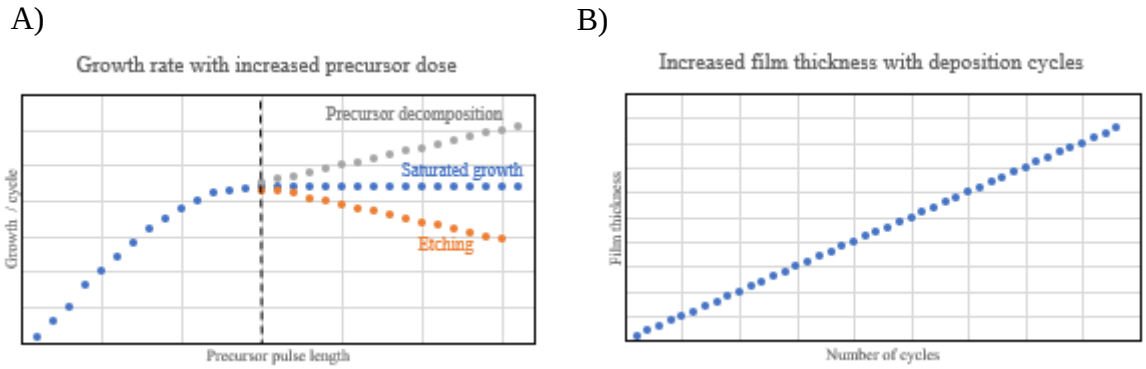

Figure 8. Illustrations of the dependency between **A)** precursor dose and growth rate, with the ideal saturated growth marked with blue dots and **B)** film thickness and number of deposition cycles in an ideal ALD process.

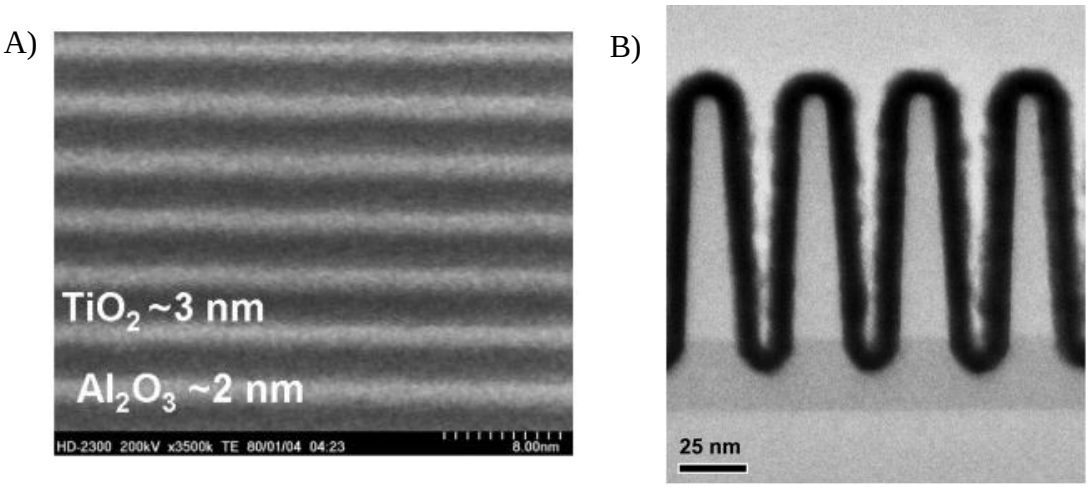

Figure 9. Structures that are possible to deposit and coat due to the unique features of ALD. **A)** Thin film nanolaminate with altering layers of TiO_2 and Al_2O_3 representing the precise thickness control of ALD.[24] Reprinted with permission from M. Laitinen, T. Sajavaara, M. Rossi, J. Julin, R. L. Puurunen, T. Suni, T. Ishida, H. Fujita, K. Arstila and B. Brijs, *Nuclear Instruments and Methods in Physics Research Section B*, 2011, **269**, 3021–3024. Copyright 2011 Elsevier. **B)** Atomic layer deposited RuO_2 layer in a trench structure representing the conformal growth of ALD.[25] Reprinted with permission from J.-Y. Park, S. Yeo, T. Cheon, S.-H. Kim, M.-K. Kim, H. Kim, T. E. Hong and D.-J. Lee, *Journal of Alloys and Compounds*, 2014, **610**, 529–539. Copyright 2014 Elsevier.

Even though ALD possesses all the positive features described above, some drawbacks are also related to the method. The main disadvantage of ALD is often considered to be its slowness.[2,3] The multi-step cycle lasts typically several seconds and grows only a maximum of one monolayer of the desired material. The slow growth can however be compensated by using as short cycle times as possible, using larger substrates and utilizing batch processing.

Additionally, efficient reactor geometry is of a great importance. In applications where film thicknesses are small the slowness is more efficiently compensated. Another limitation of ALD is the finite precursor and material selection.

ALD is used to deposit solid inorganic materials. The selection of these materials is versatile including but not limited to metals, oxides, nitrides, sulphides and fluorides.[26,27] These materials have multiple industrial applications. The first application of ALD, which is still in use, was thin film electroluminescent displays (TFEL). Other commercial applications include microelectronics, magnetic heads, protective coatings, optics, coatings on powders e.g. in catalysts, and micro electro mechanical systems (MEMS).[3] The most effective driver for the recent ALD development has been microelectronic devices. The increased interest towards ALD can be seen from the increased number of publications in the field (Figure 10).

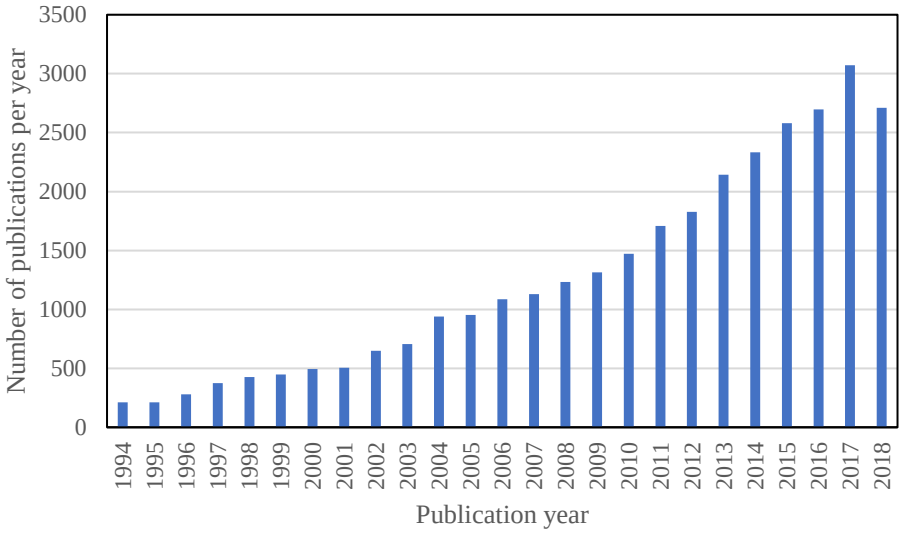

Figure 10. Number of publications in years 1994–2018 found with a search "Atomic layer deposition" from Web of Science.

The selection of metal precursors used in ALD includes for example elements, halides, alkyls, cyclopentadienyls, alkoxides, β-diketonates, alkylamides, silylamides and amidinates.[27] To ensure self-limiting surface reactions, certain criteria must be met by the ALD precursors. The key requirements to the precursors are aggressive reactivity, sufficient volatility, thermal stability and purity.[5] However, the aggressive nature of the precursors may create undesired side effects, such as reactions with the reactor components: precursor lines, valves, reaction chamber, exhaust line and pump. The precursor – reactor interactions will be more closely studied in the experimental part of this thesis.

3.2 ALD in semiconductor fabrication

As a result of the development in microelectronics industry driven by Moore's law need for new materials together with new deposition methods has risen (Figure 11). As the wafer sizes increased and the component shapes became more complex in the IC industry, key requirements for the film deposition methods started to include uniformity over large surface areas together with 3D conformality.[28] From these aspects ALD is an extraordinarily well fitting deposition method for the tightening requirements of the semiconductor industry and, in fact, microelectronics have been the major driver for the ALD development for the past 20 years.[28] The importance of ALD in technology industry was recognized in 2018 in the form of the Millennium Technology prize, awarded to Dr. Tuomo Suntola, the inventor of ALD.[29]

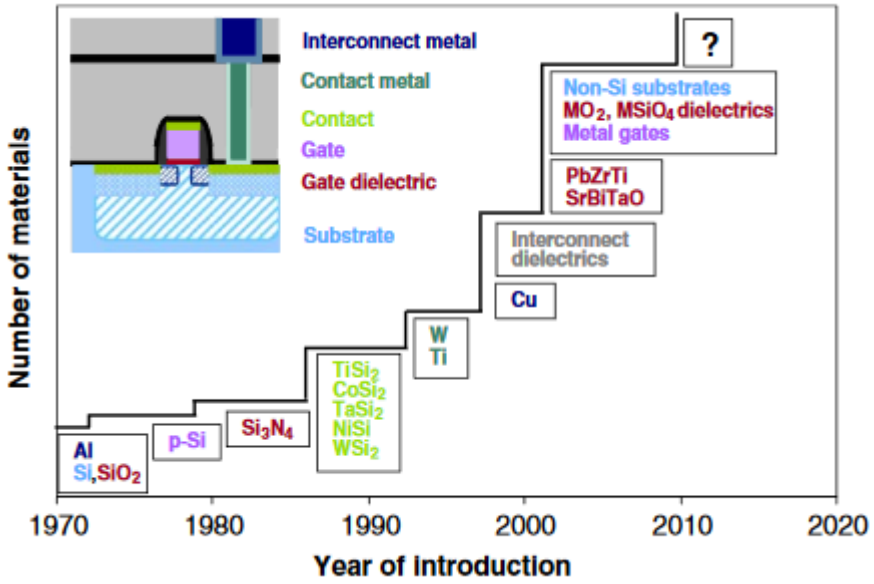

Figure 11. Widening of the materials selection in semiconductor processing.[30] Reprinted with permission from D. Hellin, S. De Gendt, N. Valckx, P. W. Mertens and C. Vinckier, *Spectrochimica Acta Part B*, 2006, **61**, 496–514. Copyright 2006 Elsevier.

Regardless of the beneficial properties of ALD also drawbacks related to its use in microelectronics industry exist. One of the biggest concerns is the relatively low throughput, which originates from the intrinsic slowness of ALD.[2,3,31] This limitation has already been at least partially solved as the film thicknesses in microelectronics have decreased into the nanometre scale. Together with the decreasing film thicknesses, batch processing is an effective way to increase throughput.[3] Other concerns of ALD are related to the high cost, limited selection of precursors and materials, and precursor residues left as impurities in the films.[2,3]

As ALD is a viable processing method for structures that utilize films in the nanometre scale, the value of ALD has been recognized only in the later IC development. In the past, the conventional deposition method has been thermal CVD.[32] Other deposition methods such as sputtering and spin coating have been used as well.[31,32] One main advantage of ALD compared to CVD is the possibility for processing at lower temperatures. Schmitz[32] states in his recent article "Several trends in microchip fabrication, – –, demand the deposition of high-quality conformal thin films at reduced temperatures."

The need for the reduced deposition temperatures is caused by the complex fabrication process of ICs, consisting of several hundred process steps with application of multiple different materials. The thermal lifecycle of an integrated circuit is presented in Figure 12. With lower deposition temperatures less diffusion and thermal expansion are observed and materials with lower melting points or decomposition temperatures can be applied. However, reduced deposition temperature tends to lead into lower growth rate and poorer film quality.[32] One way to reduce the deposition temperature is the use of plasma, e.g. in the form of plasma-enhanced ALD (PEALD, plasma-assisted ALD, PAALD).

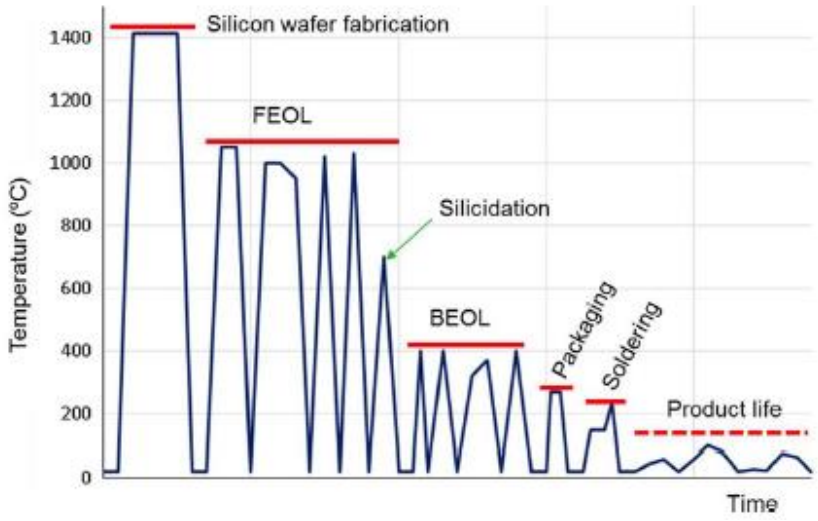

Figure 12. Temperature profile through the different fabrication steps of integrated circuits.[32] FEOL = front end of line, BEOL = back end of line. Reprinted from J. Schmitz, *Surface and Coatings Technology*, 2018, **343**, 83–88 (https://doi.org/10.1016/j.surfcoat.2017.11.013**)**, published under the Creative Commons Attribution-NonCommercial-No Derivatives License (CC BY NC ND, https://creativecommons.org/licenses/by-nc-nd/4.0/).

Three main application areas for ALD in microelectronics are memory devices, logic devices and interconnects. All these device structures utilize thin material layers in the nanometre scale. These thin material layers together with the devices themselves are vulnerable to metal contamination. Thus, in the production of these devices, contamination control is crucial.

More detailed examples of the devices are presented in chapter 3.3. Possible chemistries for the materials used in the presented applications are introduced in chapter 3.4.

3.3 Applications

The best established applications of ALD in microelectronics include the deposition of high dielectric constant (high-κ, high-k, high permittivity) materials. These materials are used as capacitor dielectrics in dynamic random access memories (DRAM) and as gate oxides in metal-oxide-semiconductor field effect transistors (MOSFET).

The definition of the relative dielectric constant is presented in Equation 2. High-κ dielectrics for DRAM and MOSFET applications have a dielectric constant in the range of 10–30 for MOSFET and even higher for DRAM.[33,34,35] The dielectric constant of silicon dioxide is 3.9,[33] which is low compared to the high-κ materials. High-κ materials for DRAM and MOSFET applications include metal oxides such as Al_2O_3, HfO_2, ZrO_2, TiO_2, Sc_2O_3, Y_2O_3, La_2O_3, Lu_2O_3, Nb_2O_5, Ta_2O_5 and their simple mixtures or nanolaminates.[28,33,34]

$$\kappa = \frac{\varepsilon_d}{\varepsilon_0} \tag{2}$$

where κ is the dielectric constant, ε_d is permittivity of the dielectric and ε_0 is the permittivity of free space.

In the semiconductor industry history, silicon dioxide (SiO_2) has been the main dielectric in use. Due to the downscaling of the device sizes, silicon dioxide thickness has been constantly decreased to maintain the device capacitance (Equation 3). However, when the silicon oxide layer thickness is decreased to only a few nanometres, tunnelling and consequent leakage currents take place, severely damaging the device performance.[2,33,34] Substitution of the silicon dioxide with high-κ materials enables the use of thicker dielectric layers thus preventing leakage currents while maintaining the capacitance (Figure 13).

$$C = \kappa \cdot \varepsilon_0 \cdot \frac{A}{d} \tag{3}$$

where C is capacitance, κ is the dielectric constant, A is the area of the device, d is the thickness of the dielectric layer and ε_0 is the permittivity of free space.

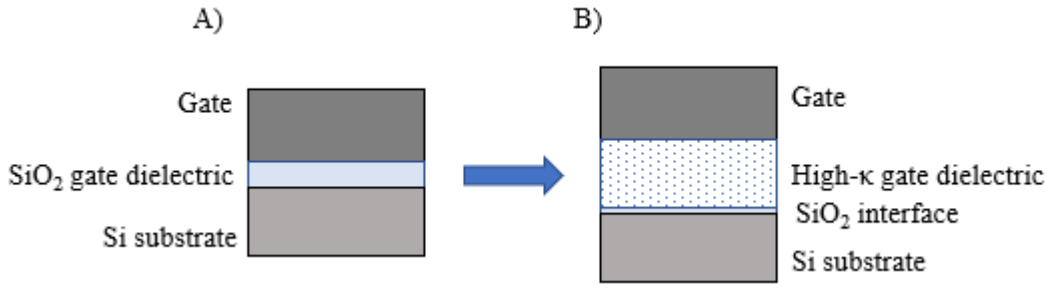

Figure 13. Change from **A)** silicon oxide gate dielectric to **B)** high permittivity gate dielectrics with larger physical thickness. Native oxide on the silicon – high-κ material interface should be calculated into the equivalent oxide thickness (EOT).

By solving Equation 3 for thickness, d, and using the κ-value of silicon dioxide, equivalent oxide thickness (EOT) can be calculated (Equation 4). EOT describes the thickness of a silicon dioxide layer that would give the same capacitance that is gained by using a high-κ material. As silicon oxidises easily, formation of a SiO_2 layer between the silicon substrate and the dielectric film affects the total equivalent oxide thickness (Equation 5). Chapters 3.3.1–3.3.2 present the use of high-κ materials in DRAM and MOSFET applications.

$$EOT = 3.9 \cdot \varepsilon_0 \cdot \frac{A}{C} \tag{4}$$

$$EOT_{tot} = EOT + d_{SiO_2} \tag{5}$$

where *EOT* is the equivalent oxide thickness, 3.9 is the dielectric constant of silicon dioxide. EOT_{tot} is the total equivalent oxide thickness and d_{SiO_2} is the thickness of the native oxide layer on silicon.

3.3.1 ALD in memory devices – DRAM

Memory devices can be divided into volatile and nonvolatile memories based on the data retention ability. Volatile memory needs constant refreshment to maintain the data, whereas nonvolatile memory can do so even when the power is cut off. Memory devices can be divided into mass-production memories including DRAM, Flash and static random access memory (SRAM) and emerging memories including e.g. magnetoresistive RAM (MRAM), resistive RAM (ReRAM) and ferroelectric RAM (FeRAM) etc. (Figure 14).

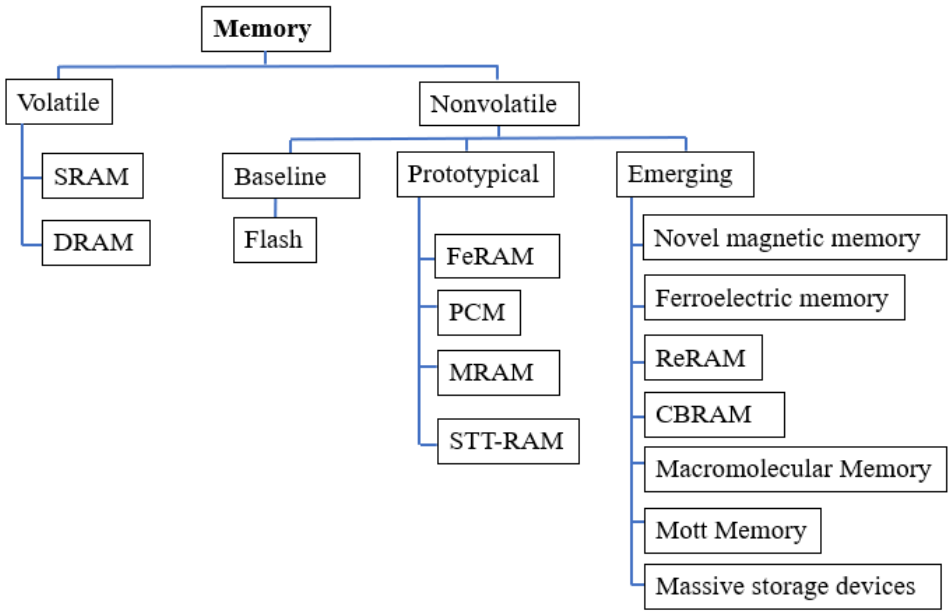

Figure 14. Categories and taxonomy of memory devices according to IRDS 2017 Beyond CMOS.[36]

Dynamic random access memory (DRAM) has a central role as a memory device utilizing the ALD technology. DRAM works as the main memory of most modern computer devices including PCs, smartphones, laptops and tablets. DRAM consists of memory cells, each of which containing a transistor and a capacitor. In DRAM fabrication ALD is applied in making the capacitors, either in the electrode deposition or when depositing a high-κ dielectric layer on top of the electrodes. A schematic presentation of DRAM and scanning electron microscope (SEM) images of DRAM capacitors are presented in Figure 15.

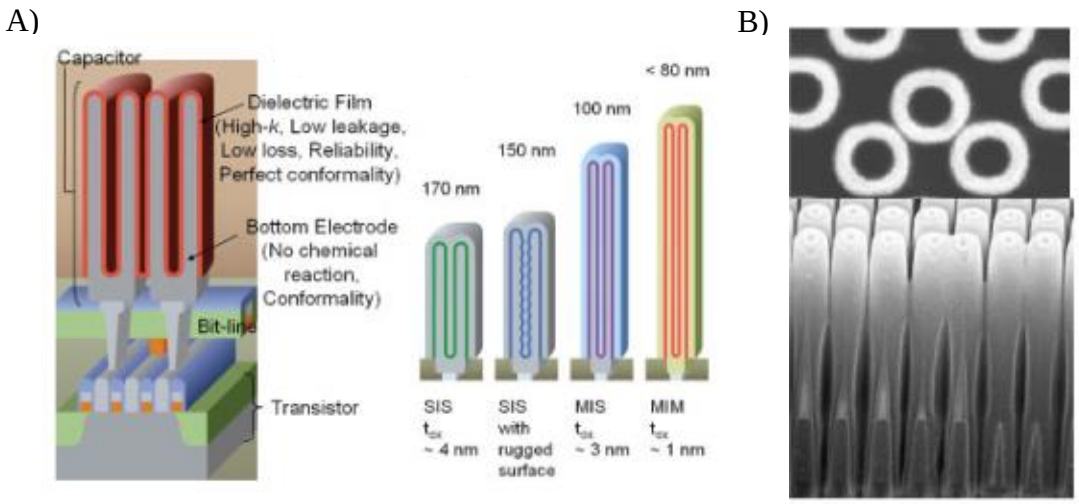

Figure 15. A) Structure and generations of DRAM capacitors.[37] Reprinted with permission from S. K. Kim, G.-J. Choi, S. Y. Lee, M. Seo, S. W. Lee, J. H. Han, H.-S. Ahn, S. Han and C. S. Hwang, *Advanced Materials*, 2008, **20**, 1429–1435. Copyright 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. **B)** Top and side view of DRAM capacitor with SEM.[17] Reprinted with permission from K. Kim, in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, IEEE, 2005, pp. 323–326. Copyright 2005 IEEE.

The high aspect ratio of the capacitor structure makes ALD a key deposition method due to its conformal growth. The latest DRAM generations have a metal-insulator-metal (MIM) structure, in which the insulator is the high-κ dielectric. High-κ dielectrics used in the capacitors include binary oxides Al_2O_3, HfO_2 and ZrO_2[17,3] and their mixtures such as Hf-Al-O.[3] A nanolaminate structure, ZrO_2-Al_2O_3-ZrO_2 (ZAZ) has been presented in the literature and is in current use.[3,35,38] Ternary oxides with a perovskite structure are new material candidates for the capacitor dielectrics as they possess κ-values over 50, which will be necessary to meet the requirements of the 35 nm generation and below.[3] Two primary oxides of interest are $SrTiO_3$ and (Ba,Sr)TiO_3.[2,3,28,35] Apart from DRAM, ALD can also be applied for other memory devices, such as NAND flash.[17,35]

As already mentioned, in addition to the dielectric deposition, ALD can be utilized in the DRAM electrode deposition. ALD has been used to deposit TiN electrode material to for example TiN/ZAZ/TiN MIM stacks.[35] CVD is a competing deposition method for TiN.[3] Another option for the electrode material is ruthenium, but the high price and problems in device integration of ruthenium make alternative materials desirable.[17,3] Platinum and nickel are other candidates.[35] Platinum is however not considered a viable electrode material due to its high cost and difficulty of etching.

3.3.2 ALD in logic devices – MOSFET

Metal oxide semiconductor field effect transistors are logic devices used in the integrated circuits, thus being present in most electronic devices such as computers. The basic building blocks of a MOSFET are source, drain, gate, gate dielectric, spacers and channel (Figure 16A). MOSFET works as a switch, allowing current to flow from the source to drain when a voltage is applied to the gate, but preventing the current flow when no gate voltage is applied. In the MOSFET structure, the source and drain can be n-type (NMOS) or p-type (PMOS) semiconductors, the substrate being doped to the opposite conductivity type (Figure 16B).

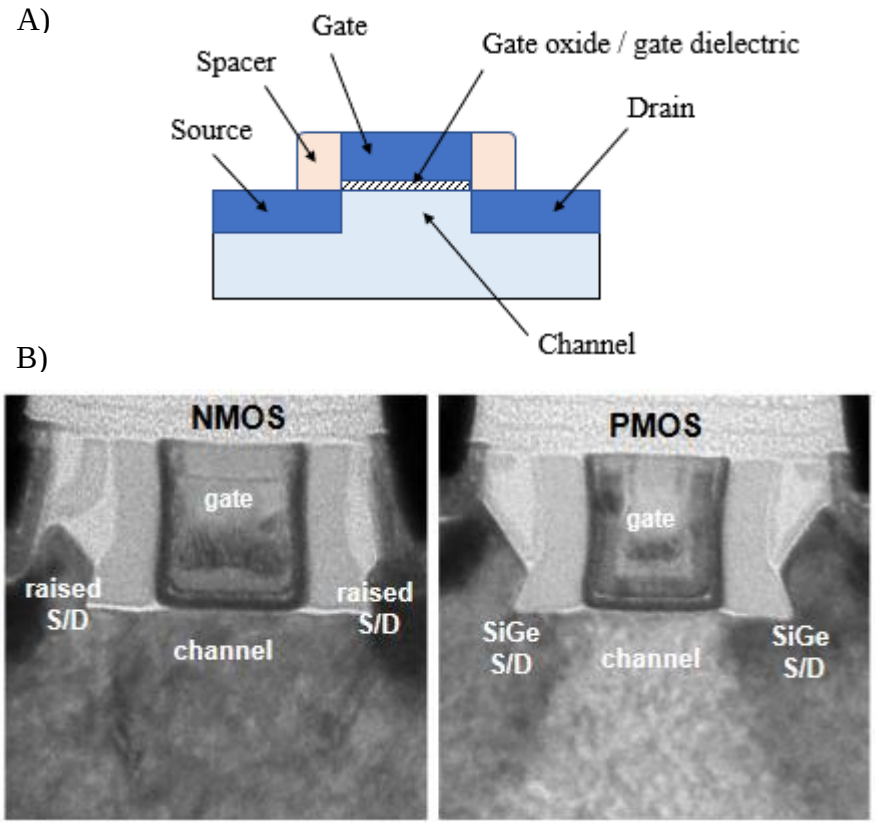

Figure 16. A) Schematic presentation of a MOSFET-structure. **B)** Cross section of NMOS and PMOS structures.[39] Reprinted with permission from P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani and O. Golonzka, in *Electron Devices Meeting (IEDM), 2009 IEEE International*, IEEE, 2009, pp. 1–4. Copyright 2009 IEEE.

Planar MOSFET structures do not depend on ALD as much as the more three-dimensional DRAMs. However, ALD is used in the MOSFET fabrication, primarily in the deposition of the gate dielectrics. Also, the more evolved logic generations have three-dimensional structures, such as FinFETs, thus favouring conformal deposition methods. Commonly used

gate dielectrics are oxides, also known as gate oxides, including Al_2O_3,[40,41] HfO_2[42,41] and ZrO_2.[2,43,44] Apart from the oxides, aluminum nitride (AlN) has been deposited with ALD[45] and by reactive molecular beam deposition[46] to function as a gate dielectric. La_2O_3, representing a rare-earth oxide gate dielectric, has been deposited with ALD.[47]

With further MOSFET development, new channel materials apart from the conventional silicon have emerged. These channel materials include germanium,[43] molybdenum disulphide (MoS_2)[40,44] and III-V compound semiconductors such as GaAs, InGaAs, InAs and InP.[48] The main motivation for the introduction of new channel materials has been the enhancement in the charge carrier velocity. However, unlike silicon, the III-V compound semiconductors do not form a native oxide layer that could be utilised as a gate dielectric.[48] Integration problems with the conventional high-κ materials have emerged as formation of a good quality interface layer has been problematic.[48,49]

One way to get around the poor interface formation is to use external interfacial layers (Figure 17). As an example, ALD deposited aluminum oxy nitride (AlON) i.e. oxidised aluminum nitride has been used as an interfacial layer between the high-κ dielectric (Al_2O_3) and III-V semiconductor channel (InGaAs).[49] Aluminum nitride has been used as an interfacial layer between ZrO_2 gate and germanium channel.[43] Additional device parts, the deposition of which has been studied with ALD include spacers[50] and metal gates.[51]

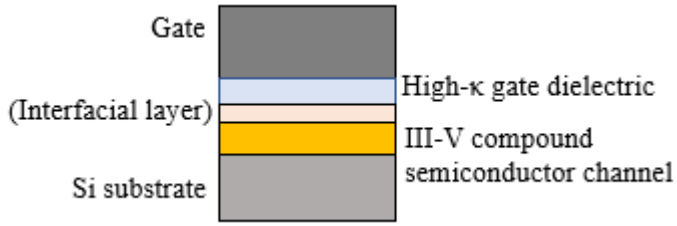

Figure 17. MOSFET structure with a gate stack composed of gate / high-κ dielectric / interfacial layer and III-V compound semiconductor channel.

3.3.3 ALD in interconnects

In integrated circuits interconnects are needed to connect the circuit components, e.g. transistors, together (Figure 18). Aluminum metal was used as an interconnect material in the past but it has been replaced by copper for enhanced conductivity. With the copper interconnects barrier layers are needed to avoid diffusion between the metal and surrounding dielectric material. In addition to the diffusion barriers, seed layers, also known as "liner" layers and adhesion layers, may be needed to guarantee high quality interconnects. With

further downscaling, all these three materials, diffusion barriers, seed layers and adhesion layers, should be conformal which makes ALD a promising deposition method.

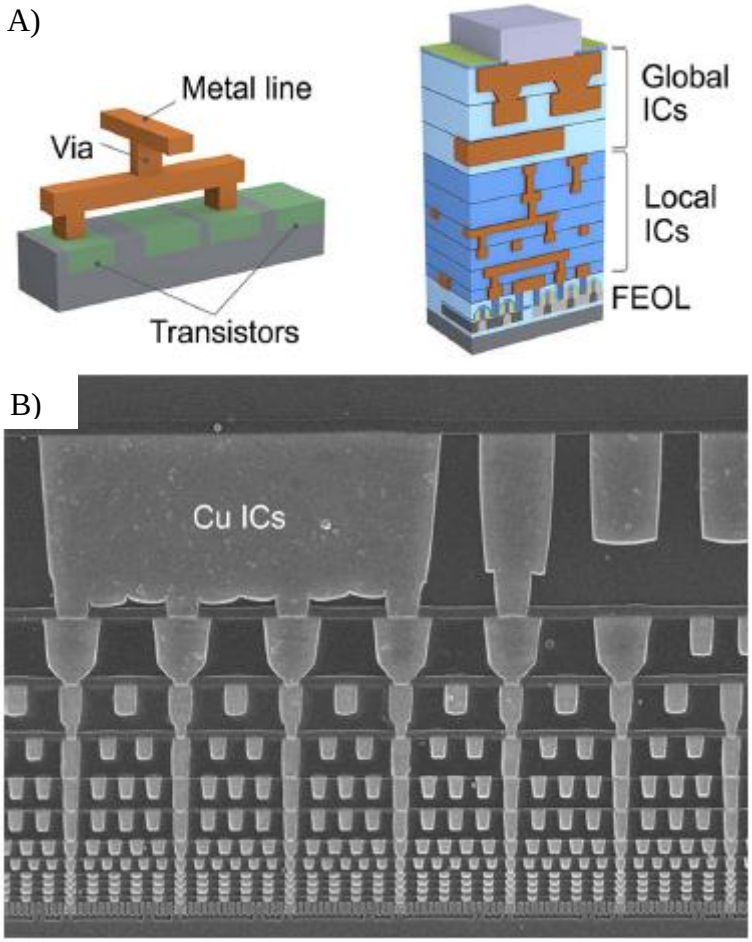

Figure 18. A) Schematic presentation of copper interconnects (brown parts in the illustration).[52] **B)** SEM picture of an Intel Broadwell structure with visible copper interconnects.[52] Reprinted from R. Bernasconi and L. Magagnin, *Journal of The Electrochemical Society*, 2019, **166**, D3219–D3225. Licensed under CC BY 4.0.

Materials used together with copper interconnects have traditionally been metals and metal nitrides.[53] ALD deposited diffusion barriers include Ta[54,55] and Ti[55] and corresponding nitrides TaN[56,57] and TiN[56] as well as WN.[58] Related to Ta and Ti based barriers, it is worth noticing that the ALD of the metallic films is significantly more challenging than the ALD of the corresponding nitride films. An additional function for the diffusion barrier layer is to promote adhesion between copper and the surrounding dielectric.[53] Apart from metals and nitrides, also oxides including Al_2O_3 and HfO_2 have been studied as diffusion barrier layers.[59] The use of ruthenium metal as an interconnect material[60] and diffusion barrier[52] has been presented. Atomic layer deposited aluminum nitride (AlN) has been studied as an interconnect capping layer.[61] Capping layers are diffusion barriers on the top surface of the

interconnects. Research on the use of ALD for the copper seed layer deposition has also been conducted.[62,63] Additionally, atomic layer deposited tungsten seed layers for tungsten plug deposition have been presented.[64] Tungsten plugs act as contacts between transistors and the network of interconnects.

3.3.4 Summary of the applications of ALD

Atomic layer deposited materials in semiconductor devices based on the academic publications presented in the previous chapters are summarised in Table 3. It is worth acknowledging that the applications of ALD in the semiconductor industry are not limited to the structures and materials presented here as most innovations in commercial applications may remain unpublished.

Table 3. Device parts possible to deposit with ALD categorized based on application. Examples of material candidates are given.

Device	**Part deposited with ALD**	**Material candidates**
DRAM capacitor	- electrode - electrode dielectric	- TiN, Ru - Al_2O_3, HfO_2, ZrO_2
MOSFET	- gate dielectric - gate - spacer - channel / gate dielectric interface	- Al_2O_3, HfO_2, ZrO_2, AlN, La_2O_3 - TiN - SiN - AlN, AlON
Interconnects	- diffusion barrier - seed, adhesion and capping layers - connective layers / plugs	- Ta, TaN, Ti, TiN, Al_2O_3, HfO_2 - Cu, AlN - W

3.4 ALD processes for semiconductor applications

The compatibility of ALD precursors with semiconductor processing is affected by several factors. Precursors should be reactive at sufficiently low temperatures, the amount of precursor residues left in the film should be low, precursors should not etch the deposited film and they should not oxidize materials that are not meant to be oxidized. As an example, when a gate oxide is deposited on top of silicon, the SiO_2 layer formation at the interface can be avoided by a careful selection of the precursors.[65] Sufficient growth rate might be a requirement as well especially when the devices are to be manufactured in high volumes.

All these parameters are chemistry and precursor dependent and the level of importance of each requirement depends on the application.

High volume manufacturing (HVM) metal precursors reported by Pegasus Chemicals, an ALD and CVD precursor manufacturer and provider, are presented in Table 4. As can be seen from the list, the precursor selection in actual use for device manufacturing is currently rather limited.

Table 4. ALD and CVD metal precursors used in high volume manufacturing according to Pegasus chemicals.

Precursor	**Chemical structure**	**Example films**
$HfCl_4$	$HfCl_4$	HfO_2
TEMAHf	$Hf(NMeEt)_4$	HfO_2
TMA	$Al(CH_3)_3$	Al_2O_3
TEMAZr	$Zr(NMeEt)_4$	ZrO_2
$TiCl_4$	$TiCl_4$	TiN, TiO_2
TDMAT	$Ti(NMe_2)_4$	TiN, TiO_2
PDMAT	$Ta(NMe_2)_5$	TaN
CCTBA/CpCoCO	$Co_2(CO)_6[HCC(CMe_3)]$ /CpCoCO	Co, CoO, Co_3O_4
silicon sources	several	Si_3N_4, SiO_2

In ALD multiple precursor chemistries may be available to deposit a film of a certain composition. However, the precursor selection strongly affects the possible impurities, quality and properties of the deposited film. Process parameters, such as deposition temperature, are also dependent on the chosen precursor chemistry. In the previous chapters, examples of possible ALD materials for microelectronics applications were presented, reflecting the importance of metal oxides and metal nitrides utilized e.g. as gate dielectrics and barrier layers, respectively. Thus, the following chapter will introduce ALD chemistries of selected metal oxides and nitrides met in chapters 3.3.1–3.3.3. With respect to the precursors the focus will be on the alternative metal sources.

3.4.1 HfO_2 processes

Hafnium oxide processes with versatile hafnium precursors together with water, ozone or oxygen plasma as oxygen sources have been presented in the literature.[66–69] The hafnium precursors can be divided into halides, alkylamides, cyclopentadienyls and heteroleptic hybrid precursors of alkylamides and cyclo-pentadienyls (Figure 19).[66] A key factor for the hafnium precursors is high thermal stability as higher deposition temperatures enhance film purity provided that no precursor decomposition occurs. From the production point of view, high growth rate is desirable. For logic applications mildly oxidizing water chemistry is preferred over strong oxidants such as ozone or oxygen plasma to avoid the undesired oxidation of the underlaying silicon substrate.[67] Due to the shortcomings of the conventional hafnium precursors, such as corrosive byproducts and poor thermal stability, there is a need for new hafnium oxide processes.

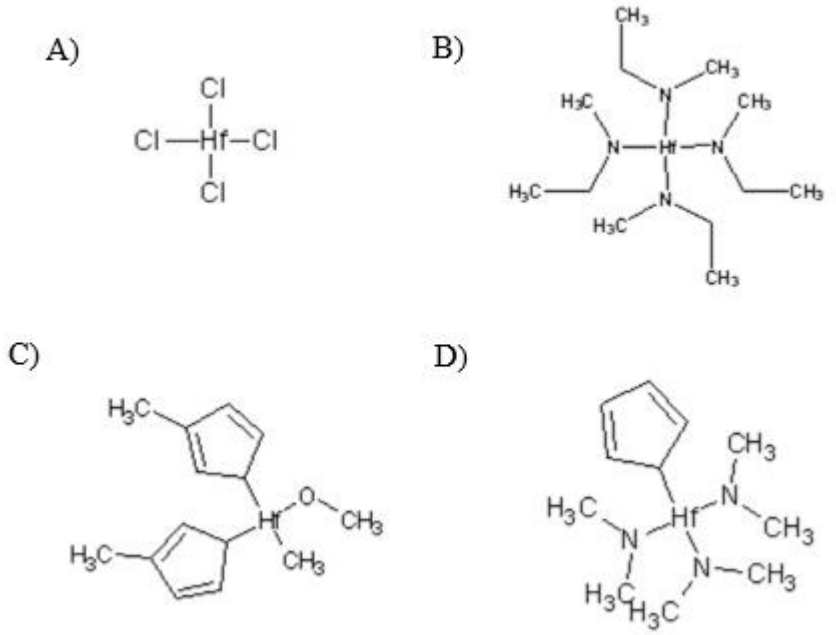

Figure 19. Structures of selected hafnium precursors. **A)** $HfCl_4$ **B)** $Hf(NEtMe)_4$ **C)** $(CpMe)_2Hf(OMe)Me$ **D)** $CpHf(NMe_2)_3$.

$HfCl_4$ is the best-established hafnium precursor from the halide group. Problems associated with this precursor include formation of corrosive byproducts (HCl), chloride impurities in the film, poor nucleation on H-terminated silicon at high temperatures,[66] and a possibility for particle incorporation because the precursor is solid.[69] However, $HfCl_4$ is a precursor used in high volume manufacturing (Table 4). Advantages of hafnium chloride include high thermal stability and lack of carbon residues in the deposited film.

Precursors from the alkylamide group include e.g. $Hf(NMeEt)_4$, $Hf(NEt_2)_4$ and $Hf(NMe_2)_4$. Benefits of these alkylamide precursors are high volatility and reactivity, resulting in high growth rate. The limited thermal stability is however a problem, resulting in increased impurity levels and poor film uniformity. The poor thermal stability of the alkylamide precursors can be avoided with heteroleptic precursors with cyclopentadienyl ligands, such as $(CpMe)_2HfMe_2$ and $(CpMe)_2Hf(OMe)Me$. However, these precursors have decreased growth rates.[66,69]

To combine the high growth rate of the alkylamides and the enhanced thermal stability of the cyclopentadienyls, hybrids of these precursors such as $CpHf(NMe_2)_3$ (HyALD^{TM}), $(CpMe)Hf(NMe_2)_3$ and $(CpMe)_2Hf(OMe)Me$ have been tailored.[66,67,69] Processes with these precursors have shown reasonable growth rates with enhanced film purity and thermal stability. Structures of selected hafnium precursors from each precursor group are presented in Figure 19. Summary of the hafnium precursors with examples is presented in Table 5.

Table 5. Summary of hafnium precursor types and examples of each group.

Group	**Examples**	**Advantages**	**Disadvantages**
Halides	$HfCl_4$, HfI_4	- high thermal stability - no carbon residues	- corrosive byproducts - halide residues in the film
Alkylamides	$Hf(NEtMe)_4$, $Hf(NEt_2)_4$, $Hf(NMe_2)_4$	- high growth rate	- limited thermal stability - H and C residues in the film
Cyclopentadienyls	Cp_2HfMe_2, $(CpMe)_2Hf(OMe)Me$	- good thermal stability	- low growth rate
Hybrides	$CpHf(NMe_2)_3$, $(CpMe)Hf(NMe_2)_3$	- good thermal stability - moderate growth rate	
Other	$Hf[OC(CH_3)_3]_4$		- poor thermal stability

3.4.2 Al_2O_3 processes

ALD chemistry of aluminum oxide is strongly focused on the trimethylaluminum (TMA) and water process. Reasons for this include the almost ideal behavior of the process, purity of the deposited films, width of the ALD window and the relatively low price of the TMA.[11] Thus, if there are no specific requirements that make the use of TMA/H_2O process unfavorable, it most likely is the process of choice. Structure of the TMA molecule is presented in Figure 20.

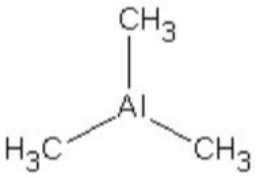

Figure 20. Structure of a TMA molecule.

Some alternative processes for Al_2O_3 have been presented in literature.[65,70] These include mostly alternative oxygen sources, such as ozone and oxygen plasma.[70] Strengths of the plasma enhanced processes include reduced cycle times, lower deposition temperatures and formation of better quality films at lower deposition temperatures. Deposition of Al_2O_3 from TMA and aluminum isopropoxide ($Al(OCH(CH_3)_2)_3$) has been presented as a method to avoid the SiO_2 interlayer formation when aluminum oxide is deposited on silicon.[65]

3.4.3 ZrO_2 processes

As zirconium and hafnium belong to the same group in the periodic table, their chemistries resemble each other. As presented by Niinistö et al.[71] and An et al.[72] zirconium oxide can be deposited with zirconium halide, alkoxide, β-diketonate, alkylamide, or cyclopentadienyl as the source. Heteroleptic precursors of alkylamides and cyclopentadienyls have been used similarly as with hafnium.[72]

Zirconium halide precursors include $ZrCl_4$[73] and ZrI_4,[74] the former being the more studied one.[71] Zirconium tert-butoxide ($Zr(O^tBu)_4$, ZTB) represents an zirconium alkoxide precursor.[75,76] Alkylamide precursors include $Zr(NEtMe)_4$ (TEMAZr), $Zr(NMe_2)_4$ and $Zr(NEt_2)_4$.[77] As with the hafnium precursors, zirconium alkylamides possess high growth rates but limited thermal stabilities. Cyclopentadienyls include $(CpMe)_2ZrMe_2$, $(CpMe)_2Zr(OMe)Me$, $Cp_2Zr(Me)_2$ and Cp_2ZrCl_2, having high thermal stabilities with reduced growth rates.[71,72,78] Heteroleptic precursors with both Cp and alkylamide ligands

include $(MeCp)Zr(NMe_2)_3$, $(EtCp)Zr(NMe_2)_3$ and $CpZr(NMe_2)_3$.[72,79] These possess high thermal stabilities and high growth rates, but are limited with a narrow ALD window.

Apart from the precursors mentioned above, research on alternative zirconium precursors has been presented. An et al. deposited ZrO_2 films by using $CpZr(NMe_2)_3/C_7H_8$ precursor as the zirconium source.[72] Huynh et al. presented precursors containing cyclic nitrogen and oxygen containing ligands with structures $ZrCp(NMe_2)_2(^iPrNCMeN^iPr)$, $ZrCp(NMe_2)(^iPrNCH_2CH_2N^iPr)$ and $ZrCp(NMe_2)(OCH_2CH_2N^tBu)$ (Figure 21).[80] The research and development of new and improved zirconium precursors with good thermal stability and film purity, high growth rate and wide enough ALD window is still ongoing.

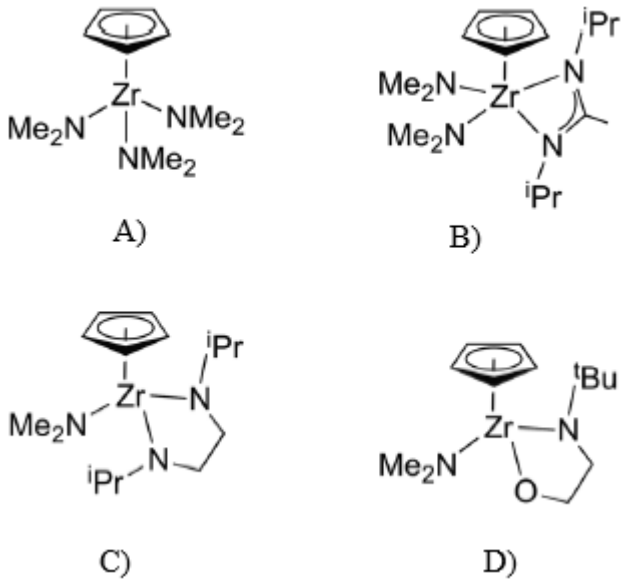

Figure 21. Zirconium precursors **A)** $ZrCp(NMe_2)_3$ **B)** $ZrCp(NMe_2)_2(^iPrNCMeN^iPr)$ **C)** $ZrCp(NMe_2)(^iPrNCH_2CH_2N^iPr)$ and **D)** $ZrCp(NMe_2)(OCH_2CH_2N^tBu)$ presented by Hyunh et al.[80] Reprinted with permission from K. Huynh, S. A. Laneman, R. Laxman, P. G. Gordon and S. T. Barry, *Journal of Vacuum Science & Technology A*, 2015, **33**, 013001. Copyright 2014 American Vacuum Society.

3.4.4 TiN processes

The main metal precursors used for the TiN deposition are $TiCl_4$[56,81] and $Ti(N(CH_3)_2)_4$ (TDMAT).[82,83] Both of these precursors are used in high volume manufacturing (Table 4). Some other precursors are presented in the literature, including the TDMAT resembling alkylamide precursor $Ti(N(EtMe)_2)_4$ (TEMAT)[84] and another halide, TiI_4.[85] The nitrogen source in the TiN depositions has mostly been ammonia (NH_3), but optional precursors such as H_2/N_2 plasma[81] and Me_2NNH_2 (DMHy)[86] have been used as well. However, both titanium precursor families have their shortcomings. Problems with the halide precursors include need of high deposition temperatures, risk of particulate contamination, chloride impurities

in the film and formation of corrosive HCl.[83] The alkylamide precursors suffer from poor thermal stability and the possibility for carbon contamination.[81]

3.4.5 TaN processes

ALD of TaN films is more complicated than the corresponding TiN films due to the difficulty of obtaining TaN with tantalum(III) instead of high resistivity Ta_3N_5 with tantalum(V). One of the most studied metal precursors for TaN deposition has been $TaCl_5$. However, the use of this precursor is problematic. The reduction power of ammonia is not sufficient to obtain TaN films from $TaCl_5$ and instead Ta_3N_5 films are obtained.[87] To compensate this problem, additional reducing agents, such as Zn[87] and TMA[88] have been used in the depositions. However, these additional reactants result in additional impurities in the films.[88] Also, the use of zinc increases the required deposition temperature as its vapour pressure is rather low and all in all Zn is not accepted in semiconductor processing.[87] Other problems with $TaCl_5$ include formation of corrosive byproduct and the possibility of particle incorporation as the precursor is solid. The use of $TaBr_5$[88] and TaF_5[89] have been studied as well, but they exhibit similar problems.

To overcome the challenges of the halides, alternative processes with metal organic precursors containing metal-nitrogen bonds have been developed. These processes include $Ta(NEt_2)_3(NtBu)$ (TBTDET) with hydrazine (H_2NNH_2),[90] ammonia[90] or hydrogen plasma.[91] Processes using $Ta(NMe_2)_5$ (PDMAT) with ammonia[92] and $Ta(NMeEt)_5$ (PEMAT) with ammonia[93] have been presented as well. Additionally, Han et al.[94] reported the use of a tantalum complex with chelating ligands, $Ta(NtBu)Me(dmaema)_2$ (dmaema = NMe_2EtNMe), together with NH_3 plasma (Figure 22).

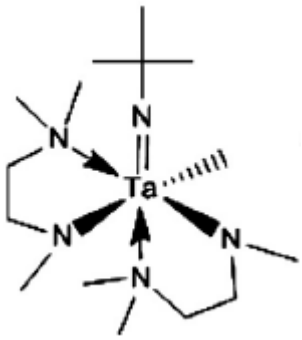

Figure 22. A tantalum complex studied by Han et al.[94] for TaN deposition. Reprinted with permission from J. H. Han, H. Y. Kim, S. C. Lee, D. H. Kim, B. K. Park, J.-S. Park, D. J. Jeon, T.-M. Chung and C. G. Kim, *Applied Surface Science*, 2016, **362**, 176–181. Copyright 2015 Elsevier.

4. Metal contamination in semiconductor industry

Even though contamination in IC production has been minimized by conducting process operations in a clean room environment with pure reagents and clean equipment, some level of contamination is inevitable. Contamination can originate from tools and equipment, chemicals, precursors, storage containers, personnel and handling of wafers. The type of contamination can vary from particles, metal traces and organics to native oxide layers and roughness.[30] Sources of contamination and different contamination types are illustrated in Figure 23.

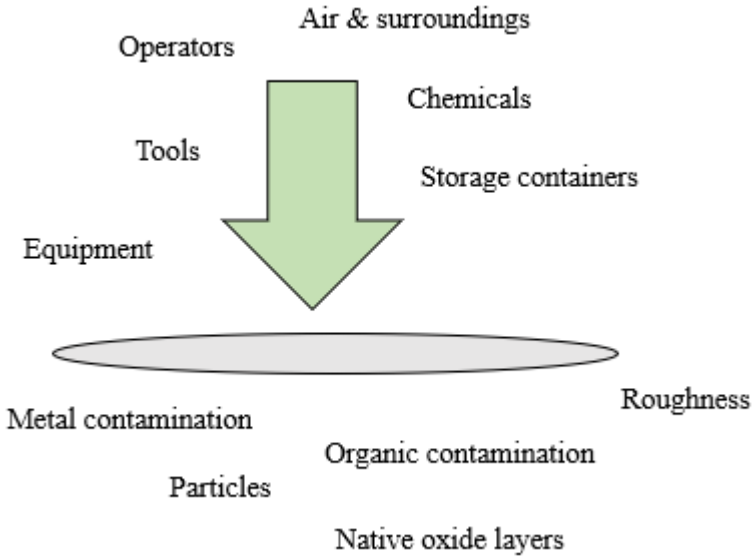

Figure 23. Contamination types and their sources.

In IC manufacturing impurities can decrease the device performance, reliability and yield. Yield is defined as the number of products made divided by the number of products that could potentially be made.[95] Over 50 % of the yield losses in integrated circuit manufacturing are caused by contamination.[4] Harmfulness of contamination is affected by its nature, location and quantity. One of the most harmful forms of contamination in semiconductor industry is metal contamination. Metal contamination can affect both the semiconductor and insulator layers of the devices. A typical feature of metal contamination is reactivity: metal species can form compounds such as silicides, silicates and oxides and they can diffuse in oxides and silicon. One critical challenge in semiconductor industry is the detection and control of a wide range of metallic impurities to enhance device performance, long time reliability and yield.

4.1 Effect of metal impurities on semiconductor devices

Metal contamination is typically measured from a wafer surface as surface contamination. Metals can be categorized into contamination classes expressing different chemistries and thus, different effects on silicon. These contamination classes are tolerated in different concentrations. International Roadmap for Semiconductors (ITRS) and International Roadmap for Devices and Systems (IRDS) have presented guidelines for these tolerable concentrations. However, these specifications are device and process step dependent. As an example, specification can be given as the maximum concentration of a metal species in a processing solution which does not tell the total amount of metal that is tolerated in the end product. Also, units of these concentrations are different, ppt versus atoms/cm^2. However, it is evident that the IC miniaturization and increasing level of process steps have led into a general trend of tightening metal specifications. Figure 24 illustrates the relationship between decreasing feature sizes and tightening metal specifications. However, it is worth noticing that the graph is somewhat outdated as the 450 mm wafer generation has not been generally applied even by 2019.

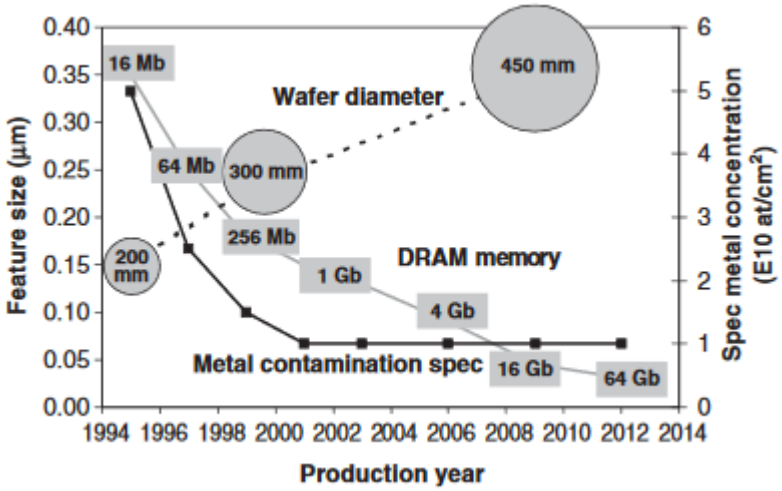

Figure 24. Evolution of metal contamination specifications with respect to DRAM generations and wafer size increasement.[30,96] Reprinted with permission from S. Pahlke, *Spectrochimica Acta Part B*, 2003, **58**, 2025–2038. Copyright 2003 Elsevier.

Contamination classes for metallic impurities based on their effects on silicon, example metals of each class and concentration level recommendations in the front end processes are presented in Table 6 according to the white paper attached to the IRDS 2017 "Yield Enhancement" report. For some applications, like image sensors, concentration limits might be more stringent than those presented in Table 6.

Table 6. Metal species as surface contaminants on silicon, allowed concentrations in the front end processes and impacts of these contaminants.[97] GOI = gate oxide integrity.

Contamination class	**Example metals**	**Allowed surface contamination (atoms/cm^2)**	**Metal impacts**
Critical GOI surface metals	Ca, Ba, Sr, Fe	$0.5 \cdot 10^{10}$	Gate oxide integrity killers
Critical other surface metals	Ni, Cu, Cr, Co, Hf, Pt	$1 \cdot 10^{10}$	Dissolve in silicon, form silicides
Mobile ions	Na, K	$2 \cdot 10^{10}$	Easily movable ions

Metal impurities are either retained on the wafer surface, or they diffuse into the silicon matrix. The main problem caused by surface impurities is degradation of the gate oxide. Impurity enhanced problems in silicon matrix include leakages at p-n junctions and dark currents in image sensors. Dark currents are undesired currents that flow through photosensitive devices when no photons are entering the device. Literature considering metal impurity effects on semiconductor devices is quite concentrated on gate oxides and their integrity.[98–101] The most often studied impurity metals are iron and copper. Istratov et al. have provided a comprehensive review on iron contamination in silicon technology.[102]

As the name implies, critical gate oxide integrity (GOI) surface metals lower the quality of the gate oxide. Thin dielectric layers are more sensitive to this degradation than thicker ones.[100] The function of the insulative layer, i.e. the gate oxide, is to prevent current flow into the gate while the current is flowing from the source to drain. Metal impurities can precipitate on the silicon – dielectric interface, diffuse into the dielectric layer or affect the dielectric growth causing its local thinning.[99,101] As an example Pan et al.[98] studied effect of various metals including Ca, Fe, Ni, Cu and Zn on the gate oxide integrity. In this study, the wafer surface was intentionally contaminated with a metal, whose effect on the electrical properties of the subsequently grown silicon oxide film was studied. Device failure was observed with Fe and Ni impurities at the level of $1 \cdot 10^{14}$ atoms/cm^2.

Metal impurities can diffuse into the silicon matrix during thermal processing or ion implantation.[103] Additionally, they can form metal silicide precipitates acting as defects. In the bulk silicon metal impurities cause junction leakages[104] and dark currents in CMOS image sensors.[105] Distribution of the metals in the wafer depends on their diffusion coefficients in silicon and in the dielectric layer.

Ionized metallic contamination, including Na^+, K^+ and Li^+, are contaminants in the dielectric layer that drift under the influence of an electric field. In the wafers these contaminants can cause various "drift effects" including e.g. drift currents, unstable surface potential and surface leakage currents, resulting in reliability problems in the semiconductor devices.[106,107]

Apart from the classification described above, metallic contaminants are often divided simply into heavy metals and alkali metals (Table 7).[4] Heavy metals are typically considered the most critical elements for semiconductor device performance. This metal class includes copper and iron, the most typical examples of harmful metal contaminants. Heavy metal contamination leads into an introduction of energy states in the semiconductor band gap which in turn results in carrier lifetime degradation and increased junction leakage currents. Examples of other degradation mechanisms, partially already discussed in the previous chapters, are presented in Table 7.

Table 7. Metals organized based on the level of their harmfulness in silicon devices as presented in "Overview and Evolution of Silicon Wafer Cleaning Technology".[4]

Level of harmfulness	**Elements**	**Device degradation mechanisms**[108]
Most critical (heavy metals)	Cu, Fe, Ni, Cr, Co, Mo	- junction leakage currents - carrier lifetime degradation - gate dielectric degradation
Critical (alkali metals)	Na, K, Li, Ca	- gate dielectric degradation - threshold voltage shift - variations in surface potential - local distortion of electric field
Least critical (other metals)	Al, Mg	- increase in interface states

Metal classes and their harmfulness presented above considered metal impurities in silicon-based devices. However, devices based on other semiconductor materials such as III-V compound semiconductors are emerging as they are utilised in the More than Moore based applications and in other applications such as high electron mobility transistors (HEMT). These compound semiconductor materials include e.g. GaN, GaAs, InP, InAs, InGaAs and GaSb. Literature considering metal contamination in compound semiconductors is limited to total reflection X-ray fluorescence spectroscopy (TXRF) and time-of-flight secondary ion mass spectrometry (TOF-SIMS).[103,109,110]

Due to the decrease in the tolerated metal impurity concentrations in semiconductor processing, metal concentrations need to be controlled and analysed at lower levels. Thus, detection methods that are reliable and highly sensitive to the metals in question are required. The complexity of the analysis is increased by a small sample volume, high matrix concentration and ultra-trace measurement levels. Introduction of new materials into the devices increases the number of metals that need to be analysed. Additionally, as already mentioned, metal impurities in the III-V compound semiconductor surfaces need to be controlled as well, which sets new requirements for the analysis.

4.2 Quantitative analysis of metal contamination on surfaces of silicon wafers

The evolution of semiconductor industry has set new requirements for the methods used in metal contamination analysis from wafer surfaces. Three major factors causing the need for more advanced methods have been the introduction of new materials to the semiconductor devices, increasing substrate sizes and increasing demand in the sensitivity.[30] The most frequently applied techniques include total reflection X-ray fluorescence, inductively coupled plasma mass spectrometry (ICP-MS) and graphite furnace atomic absorption spectrometry (GF-AAS).[30,111,112] These methods are typically combined with a sample preparation method called vapour phase decomposition and droplet collection (VPD-DC, VPD).[30,113] A desirable analysis method for the surface contamination would be sensitive to all analytes of interest, have low detection limits and it would be fast and robust with the ability to determine multiple elements simultaneously.

4.2.1 Vapour phase decomposition

The aim of VPD as a sample preparation method is to concentrate all the analytes from a silicon wafer surface into one extraction droplet that is then analysed. The analysis is divided into sequential steps which are demonstrated in Figure 25. The first step is the decomposition of the surface oxide layer with condensed HF vapour to transfer the analytes from a solid to a liquid phase (Equations 6–7).[114] Metals that are more electronegative than silicon e.g. Cu, Ag, Au and Pt can reduce back to a solid form i.e. “plate” onto the wafer surface (Equation 8).[114] These metals are dissolved back to the liquid phase by adding highly oxidative agent such as hydrogen peroxide (H_2O_2) into the extraction droplet (Equation 9).[114] The exposed hydrophobic wafer surface is scanned with this extraction droplet, thus collecting all the metal impurities into the droplet. If the analysis is done from a liquid phase, which is the case with the ICP-MS and AAS methods, the extraction is followed by the

analysis. If VPD is combined with a solid state analysis method such as TXRF, the extraction droplet is dried onto a solid surface and the analysis is carried out from the solid residue.

$$SiO_2(s) + 4\ HF\ (aq) \rightarrow SiF_4(aq) + 2\ H_2O\ (l) \quad (6)$$

$$CuO(s) + 2\ HF\ (aq) \rightarrow CuF_2\ (aq) + H_2O\ (l) \quad (7)$$

$$2\ CuF_2(aq) + Si\ (s) \rightarrow SiF_4\ (aq) + 2\ Cu\ (s) \quad (8)$$

$$Cu(s) + 2\ HF\ (aq) + H_2O_2\ (aq) \rightarrow CuF_2\ (aq) + 2\ H_2O\ (l) \quad (9)$$

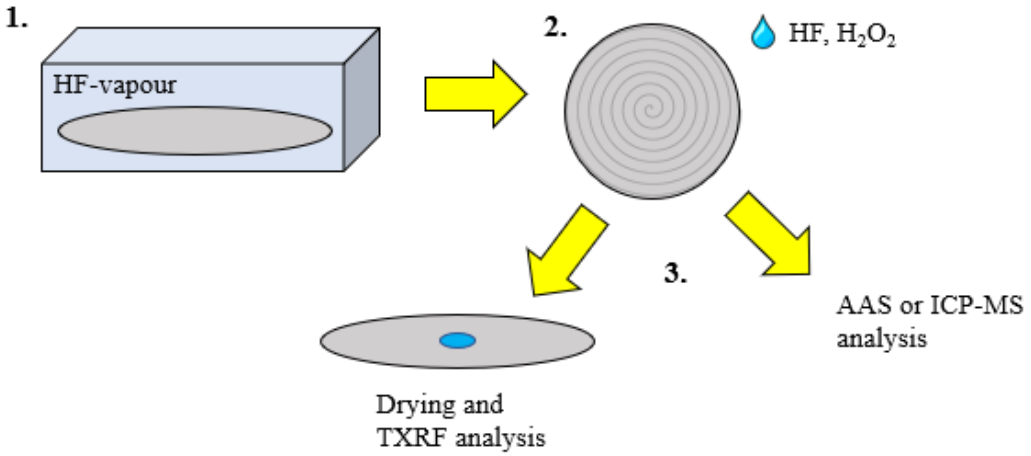

Figure 25. Schematic presentation of VPD. Steps: **1.** Decomposition of silicon oxide with HF vapour, **2.** Scanning of the surface with an extraction droplet, **3.** Analysis or drying and analysis.

One essential advantage of VPD as a sample preparation method is the concentration of the analytes into a single droplet. Collection of the metal contaminants from the whole surface area of the wafer results in higher metal concentrations in the analysis droplet and makes the detection of the analytes easier. This is valuable due to the detection limits of the analysis methods combined with the need to meet the stringent requirements of the metal impurity concentrations. Scanning of the whole surface area also increases the representativity of the analysis and makes it statistically more valid. If measurements would be done locally from single measurement points, the number of data points should be increased with increasing wafer size to keep the measurement representative. As Hellin et al.[30] stated in their review paper, in a five-point TXRF measurement on a 150 mm silicon wafer the analysed surface area is approximately 1.4 % of the total area. On a 300 mm wafer this would be only 0.35 %. Increasing the number of the measured data points becomes laborious as the wafer sizes increase but scanning of the wafer surface solves this problem.

As a downside, wafer scanning results in a loss of local information and makes practical contamination mapping impossible. Sample preparation inevitably makes analysis more laborious and lengthens the turnaround time. Another key issue with VPD is the recovery of the metals from the dissolved liquid phase to the extraction droplet. The recovery is different for different metals and can be affected by the composition of the extraction medium.[30,115] Especially the recovery of copper has shown to be incomplete, which might cause problems as copper is one of the most harmful metal impurities in the semiconductor applications.[112,116] Example recoveries for different metals with a $HF/H_2O_2/H_2O$ extraction medium are presented in Figure 26. As VPD involves the decomposition of the wafer surface, the method is destructive.

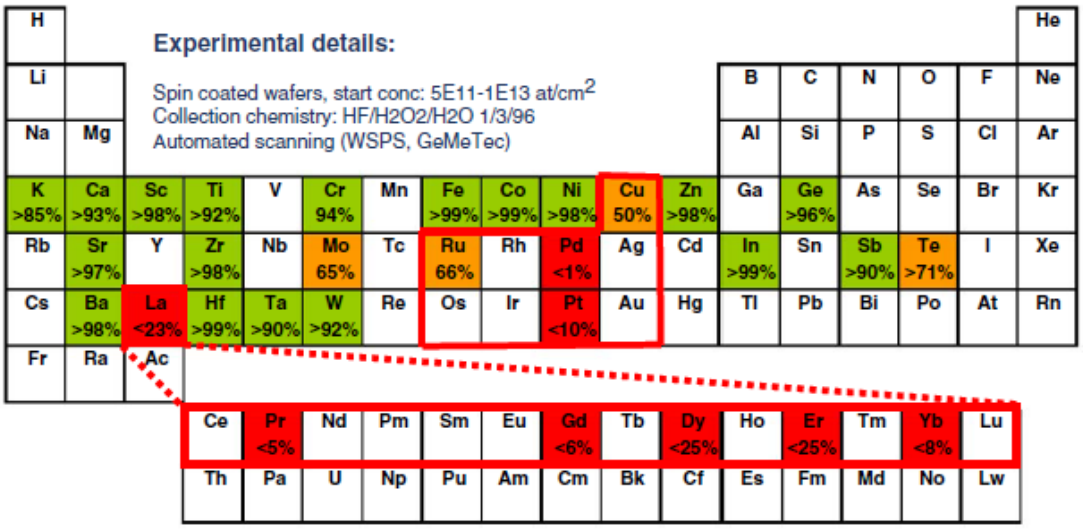

Figure 26. Recoveries of different metals with $HF/H_2O_2/H_2O$ extraction medium.[30] Reprinted with permission from D. Hellin, S. De Gendt, N. Valckx, P. W. Mertens and C. Vinckier, *Spectrochimica Acta Part B*, 2006, **61**, 496–514. Copyright 2006 Elsevier.

4.2.2 Total reflection X-ray fluorescence

A schematic illustration of TXRF measurement is presented in Figure 27. The incident angle of the X-ray beam to the sample, here marked with theta (θ), is below a radiation source and sample dependent critical angle, which results in a total reflection of the beam from the sample surface. Due to the small angle of the incident beam, the X-ray radiation penetrates only the first couple of nanometres of the sample surface. This limits the background signal originating from the matrix to the minimum and makes the detection of surface contaminants possible. When the X-ray radiation enters the sample surface it removes inner shell electrons from the sample atoms, causing excited states. Relaxation of these excited states occurs when

outer shell electrons fill the holes left by the removed electrons. This relaxation process results in atom characteristic fluorescence radiation, which is detected and analysed.

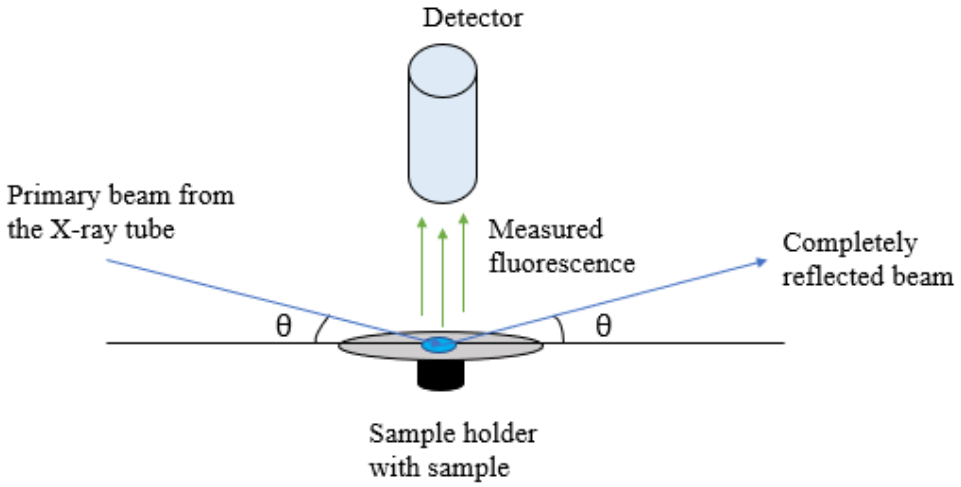

Figure 27. Schematic presentation of a TXRF measurement.

One advantage of the TXRF analysis is that it does not necessarily require sample preparation. If the measurement is carried out directly from the silicon wafer, the analysis is non-destructive. However, as discussed above, when the impurity concentrations are extremely low and the wafer sizes are large, direct TXRF measurements are not applicable due to the insufficient limit of detection (LOD) values and the lack of representativity of single spot analysis. Analyte concentrations can be enhanced by utilizing VPD with TXRF, but this increases the required work and makes the analysis destructive. Issues related to the drying of the extraction droplet after VPD have been reported.[117,118] VPD-TXRF suffers from a saturation effect, which means that metal impurity concentrations are underestimated, especially at high concentrations.[30] Thus, if VPD sample preparation is required, wet chemical methods like ICP-MS and AAS start to compete with TXRF. Additional difficulties in the TXRF analysis include problems in finding an X-ray source that can excite all elements of interest simultaneously. This problem has been solved by using multiple X-ray tubes with different energies.[30]

4.2.3 Inductively coupled plasma – mass spectrometry

Fundamental parts and the basic principle of ICP-MS are illustrated in Figure 28. ICP-MS tool consists of the same parts as any mass spectrometer, but with the specification that the ion source is inductively coupled argon plasma. The sample is introduced into the system in a liquid form and nebulized with argon gas. Argon is also used as a carrier gas when the sample is introduced into the plasma. Inductively coupled plasma is used to vaporize and ionize the sample, after which the ions are directed to a mass analyser. The mass analyser separates the ions and transfers them to the detector.[119] In general ICP-MS is frequently used in elemental analysis.

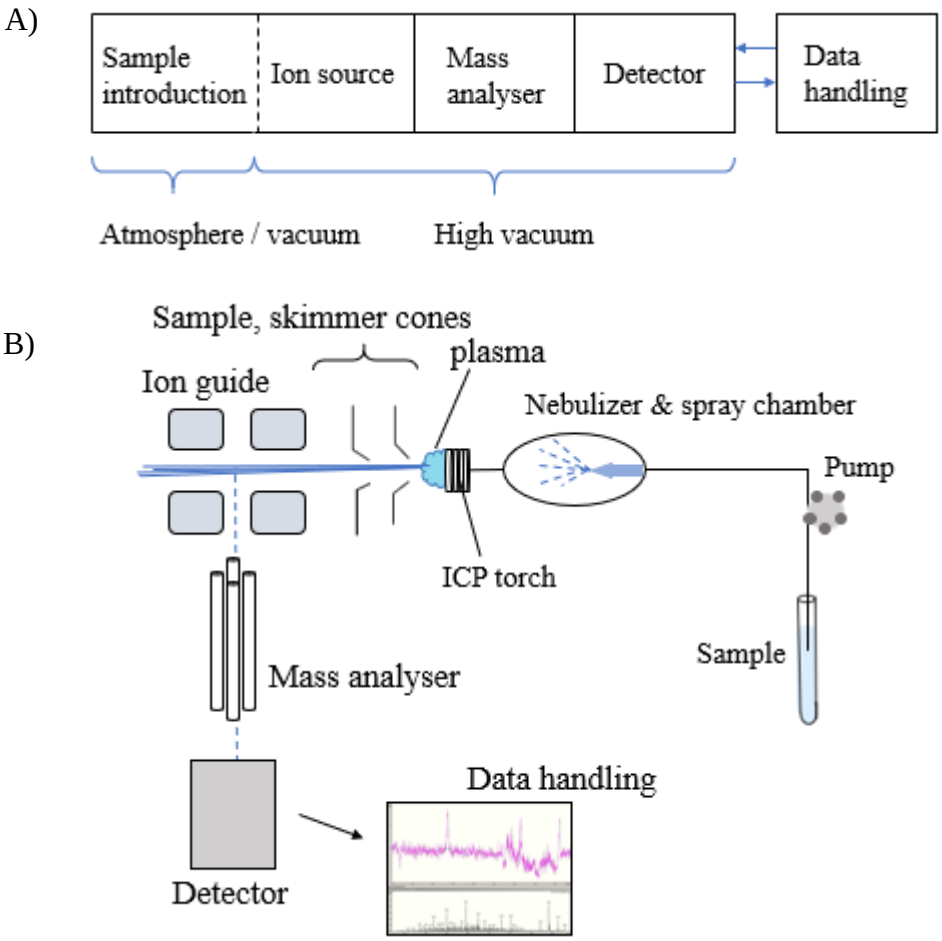

Figure 28. A) Main components of an ICP-MS instrument.[119] **B)** More detailed sketch of the ICP-MS system.

In the surface contamination analysis AAS and TXRF have been the methods of choice in the past, but as the sensitivity requirements have increased ICP-MS has gained attention as an alternative analysis tool.[112] The strengths of ICP-MS include sensitivity and good elemental coverage over the whole periodic table.[112,120] Most academic publications related

to trace metal analysis on silicon surfaces with ICP-MS originate from the 1990s and only a few papers have been published since.[112,120,121,122] However, presentations and information sheets from the analysis equipment providers, such as Agilent, Perkin Elmer and Thermo Fisher are available.[114,123,124,125] A reason for the lack of academic publications might be that ICP-MS related research and development is carried out inside semiconductor companies who do not publish the results.

The strengths of ICP-MS as stated by Agilent include sensitive analysis of 40 elements in one run with a turnaround time of 20 minutes, including the sample preparation.[114,123] Most difficulties in the ICP-MS analysis are related to the sample preparation, including small sample sizes and possible contamination of the sample during the preparation. Strictly ICP-MS related problems include interferences from molecular ions and high background equivalent concentrations.[119,120,122] Molecular ions interfering with the analytes originate from the presence of argon, the nebulizing gas, and silicon, the sample matrix. As an example, $^{40}Ar^{16}O$ interferes with ^{56}Fe and $^{30}Si^{16}O$ interferes with ^{46}Ti.[120,122] Fluoride, originating from the VPD gas and extraction solvent can also cause formation of interfering molecular ions, such as $^{40}Ar^{19}F$ interfering with ^{59}Co.[120,122] Conventional quadrupole mass spectrometers lack the resolution to separate these interference peaks, which must be compensated by using high resolution ICP-MS. Another option is to use cold plasma or dynamic reaction cell together with quadrupole MS.[120] The requirement for these special features raises the price of the analysis tool.

4.2.4 Graphite furnace atomic absorption spectrometry

GF-AAS is a method based on the characteristic absorption energies of different elements. When metal contamination is measured, the analysis is done from a liquid phase. The sample droplet is positioned inside a graphite furnace which is then heated. The heating is done in a stepwise manner and the phases can be divided into drying, pyrolysis, atomization combined with the absorption measurement, and cleaning of the furnace (Figure 29B). During the atomization, the sample is exposed to light which the metal atoms absorb at their characteristic wavelengths. After passing the atomized gas, light goes through a monochromator which selects the wavelength at which the element of interest absorbs and directs it to a detector (Figure 29A). The concentration of the analyte is determined by comparing the measured absorbance with a calibration curve. Due to the operational principle of GF-AAS, only one element can be measured at a time.

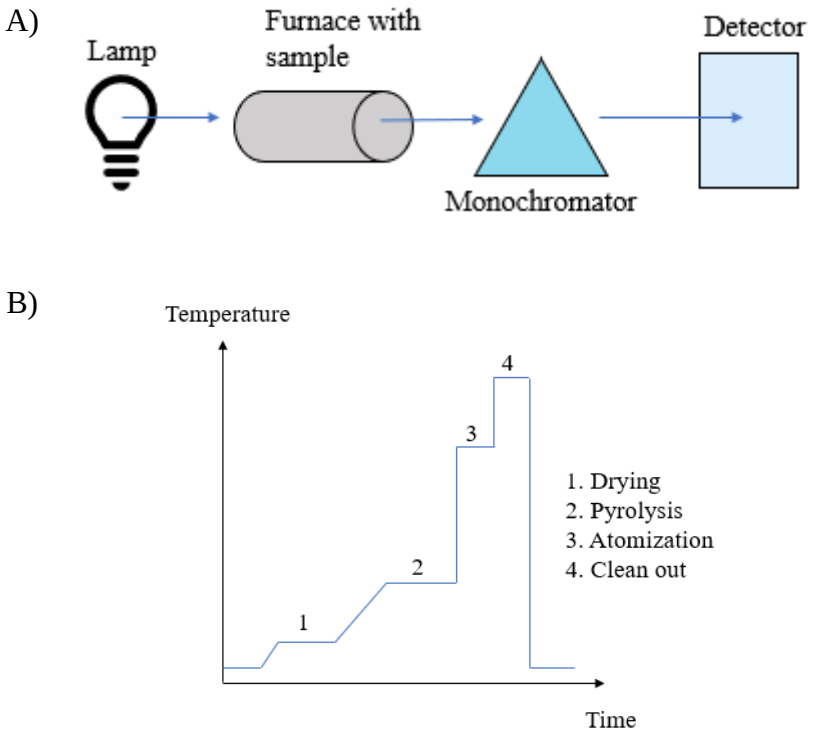

Figure 29. A) Schematic presentation of the analysis method. **B)** Step-wise heating of the sample in graphite furnace.[126]

GF-AAS has been used for the metal contamination analysis alongside TXRF and ICP-MS in the past.[127,128] However, AAS was found to be unpractical already in the 1990s.[121] The main reason for this is the inevitable slowness of the method, as only one element can be analysed at a time. Also, the common drawbacks related to liquid phase analysis from silicon wafers apply to GF-AAS as well. Advantages of the method include relatively low price of the analysis tool, simplicity of the analysis, and that the method is well known due to its long history. These advantages are not enough to compensate the inefficiency of the method in commercial field, where ICP-MS and TXRF are used as the main analysis methods. Other analytical methods applicable to metal contamination analysis of silicon wafers include TOF-SIMS[129] and synchrotron radiation TXRF (SR-TXRF).[130]

4.2.5 Summary of the analytical methods

Strengths and weaknesses of the typical methods for the analysis of metal contamination on silicon wafer surfaces are summarised in Table 8.

Table 8. Strengths and weaknesses of the typical methods for the analysis of metal contamination on silicon wafer surfaces.

Method	Advantages	Disadvantages
TXRF	- No sample preparation - Non-destructive - Contamination mapping possible	- Less sensitive - Single point measurements
VPD-TXRF	- More sensitive that TXRF - Whole wafer analysed with one measurement	- Destructive - Requires sample preparation - Problems related to drying of the sample droplet
ICP-MS	- Sensitive - Multielement analysis	- Destructive - Requires sample preparation - Expensive equipment
AAS	- Low-cost equipment	- Single element analysis at a time - Destructive - Requires sample preparation - Slow

5. Interactions of ALD precursors with oxidized metal surfaces

It is important to understand the chemistry between the parts of the ALD reactor and the ALD precursors, as the interaction between these two can affect the deposited film. The metal parts of the reactor, such as the reactor chamber, are either oxidized from the surface due to exposure to air and moisture or coated with atomic layer deposited metal oxides. Thus, the topmost surface is a metal oxide layer, capable of reacting with the precursors pulsed into the chamber. Possible reactions include e.g. etching of the metal oxide by the ALD precursors and conversion reactions that release new metal components to the gas phase. These metal components may be further transported to the substrate as metal impurities.

One example of precursor interactions with solid materials is etching reactions. During atomic layer deposition the already deposited film can be etched by the metal precursor itself (Equations 10–12).[131] Self-etching may occur especially when metal halides such as metal chlorides and fluorides are used. The film etching is based on the formation of volatile metal halide or metal oxyhalide products. In a typical ALD process, these etching reactions can result in increased nonuniformity of the deposited film or prevent the film growth completely.

$$3\ NbCl_5\ (g) + Nb_2O_5\ (s) \rightarrow 5\ NbOCl_3\ (g) \quad (10)[132]$$

$$MoCl_5\ (g) + Mo\ (s) \rightarrow 2\ MoCl_{5-x}\ (g) \quad (11)$$

$$WF_6\ (g) + 2\ WO_3\ (s) \rightarrow 3\ WO_2F_2\ (g) \quad (12)[133]$$

Apart from the self-etching reactions, etching of metal oxides can also occur by a metal halide consisting of another metal than the oxide i.e. through conversion reactions (Equations 13 and 14). Ritala et al.[65] presented etching mechanism in Equation 14 to take place when mixed-oxide films were deposited from metal halides and metal alkoxides. Corresponding etching mechanism can also take place e.g. in a nanolaminate deposition. Apart from metal halide precursors, also other precursors can cause etching. As an example, Elam et al. have presented etching of zinc oxide (ZnO) with TMA (Equation 15) when depositing ZnO/Al_2O_3-laminate structure.[134] These conversion reactions release new metal components to the gas phase and might cause problems in thickness and composition control.

$$4\ AlCl_3(g) + 3\ TiO_2(s) \rightarrow 2\ Al_2O_3\ (s) + 3\ TiCl_4\ (g) \quad (13)$$

$$HfCl_4(g) + TiO_2(s) \rightarrow HfO_2\ (s) + TiCl_4\ (g) \quad (14)[65]$$

$$2\ Al(CH_3)_3(g) + 3\ ZnO\ (s) \rightarrow Al_2O_3\ (s) + 3\ Zn(CH_3)_2\ (g) \quad (15)$$

Equations 16 and 17 have been presented in a paper by Soininen et al.[135] where $Sr(thd)_2$ was used as an in situ synthesized precursor to deposit strontium sulfide (SrS). The in situ preparation of $Sr(thd)_2$ is based on the reaction between the protonated ligand (Hthd) and strontium metal or strontium oxide. This sets an example of a reaction where a precursor ligand acts as the etching agent.

$$2\ Hthd\ (g) + Sr\ (s) \rightarrow Sr(thd)_2\ (g) + H_2\ (g) \quad (16)[135]$$

$$2\ Hthd\ (g) + SrO\ (s) \rightarrow Sr(thd)_2\ (g) + H_2O\ (g) \quad (17)[135]$$

thd = 2,2,6,6-tetramethyl-3,5-heptanedionato

Several factors can affect the probability of the reactions presented above. These include for example the reactivity of the gaseous reactant, which in the case of good ALD precursors is supposed to be high. Another factor is the stability of the solid surface being etched, the more stable solids being less likely to be etched. One factor is also the volatility of the reaction product. The equilibrium of these reactions is affected by the gas flows in the ALD reactor, as gas flows continuously towards the exhaust and thus removes the reaction products from the system. With volatile byproducts this favors the etching reaction. The feasibility of the reactions can be estimated with the change in Gibbs free energy (ΔG), more negative ΔG corresponding to a more spontaneous reaction.

If reactions resembling those presented in Equations 10–17 take place in the ALD reactor between a precursor and the reactor surface, metal impurities can be transferred from the construction metal to the processed samples. As already mentioned, metal surfaces in ALD reactors have been exposed to air and thus even the uncoated metal parts contain a native oxide layer which can be etched. Similarly, when a protective coating is applied on top of the metal surface of the reactor, the protective layer can be etched by the ALD precursors.

6. Corrosion protection with ALD

Corrosion is defined as a chemical or electrochemical reaction of a material with its environment, which leads into detrimental effects to the usage of the material.[136] Corrosion is a wide and expensive problem in the modern society. Its global annual cost is evaluated to be 2.5 trillion U.S. dollars (2.2 trillion €), which corresponds to approximately 3.4 % of global gross domestic product (GDP).[137] Corrosion has various forms as the corroded material can vary from metals to plastics, and the corrosive agent may be in the form of gas, liquid, solid or plasma. Applications in which corrosion is problematic are versatile as well, ranging from infrastructure and hardware, like vehicles and bridges, to small devices including for example lithium-ion batteries, light emitting diodes (LEDs) and transistors.[11]

There are multiple methods to prevent corrosion, one of which is the use of barrier coatings. The basic idea of a barrier layer is to prevent the access of corrosive agents to the protected surface. One attractive method for barrier layer formation are thin film techniques. Methods utilized for protective thin film deposition include e.g. sol-gel, physical vapor deposition, chemical vapor deposition and atomic layer deposition.[138,139,140] Strengths of ALD in corrosion protection are good uniformity over large areas, ability for batch processing, conformality and high film quality.

The most utilized ALD coating, also in corrosion protection, is aluminum oxide. As Salmi[11] states, the main reasons for favoring Al_2O_3 are the ideal behavior of the TMA/H_2O process, width of the ALD window, amorphous nature of the films below 800 °C and low price of the precursors. As a downside, Al_2O_3 dissolves into both, acids and bases. One special feature related to metals and their protection against corrosion is the conformal and self-healing native oxide layer formed on top of the metal surface due to surface oxidation. Native oxides and their corrosion resistances differ between different metals and one way to strengthen the corrosion resistance of a metal is the use of alloys. However, external protective coatings are applied as well. Corrosion protection of different metals with various ALD deposited thin films and nanolaminates, especially with oxides, are presented in literature. Apart from Al_2O_3 frequently utilized oxide coatings include TiO_2, Ta_2O_5, SiO_2, ZrO_2, ZnO and HfO_2.[11] Nitride coatings, mostly used as diffusion barriers include TiN, TaN, WN, NbN, MoN and VN.[11]

The capability for corrosion prevention is often tested by immersion tests, where the coated substrate is exposed to a vigorous media such as NaCl solution. In the following chapters,

the focus is on the corrosion protection towards gaseous corrosives, as the ALD reactor is exposed to gases. Additionally, the focus is given to protection of metal surfaces, as the typical construction materials of ALD reactors are metals. Apart from passivating films against corrosion, also diffusion barriers are discussed, as the diffusion of metallic species through the passivating film might lead into a transport of metallic species into the gas phase. Corrosion inside a coated and uncoated ALD reactor is illustrated in Figure 30.

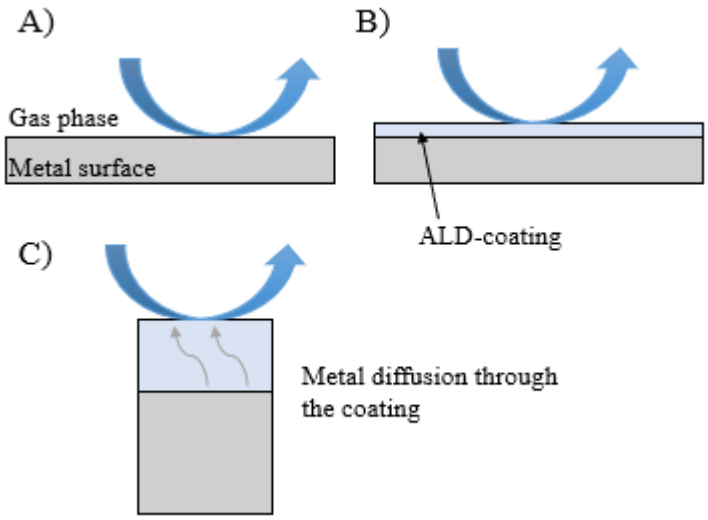

Figure 30. Possible ways for corrosion in an ALD reactor. **A)** Corrosion of an uncoated metal surface. **B)** Corrosion of the ALD coating on top of the metal surface. **C)** Diffusion of metal species through the protective layer causing corrosion of the metal alone or together with the coating.

6.1 Protection against gaseous corrosives

Regarding gaseous corrosives, barrier coatings have been mostly used for protection against atmosphere i.e. oxygen and moisture. Typical application areas for these moisture barriers have been plastics in food packaging and thin film encapsulation (TFE) of organic devices, such as OLEDs.[11,141] ALD coatings on metals against gas phase corrosives have been applied on nanoparticles,[142] nanoparticle catalysts,[143] plasmonics[144] and directly on a bulk metal surface.[145] Protection of silver surfaces for example in jewelry against visually unpleasant tarnishing has been achieved with ALD (Figure 31B).[146,147] Tarnishing of silver occurs due to a formation of chemical compounds, such as Ag_2S, when silver is exposed to moist air. The contact of silver with air can be prevented with a thin metal oxide layer that does not significantly change the visual appearance of the silver object (Figure 31C). Recent literature presents a similar application, passivation of plasmonic colors on bulk silver, with ALD aluminum oxide.[148] Plasmonic colors are colors created by interaction of light with

nanostructured metal surfaces. The effect of ALD coating in preventing the tarnishing of plasmonic colors on silver is presented in Figure 31A.

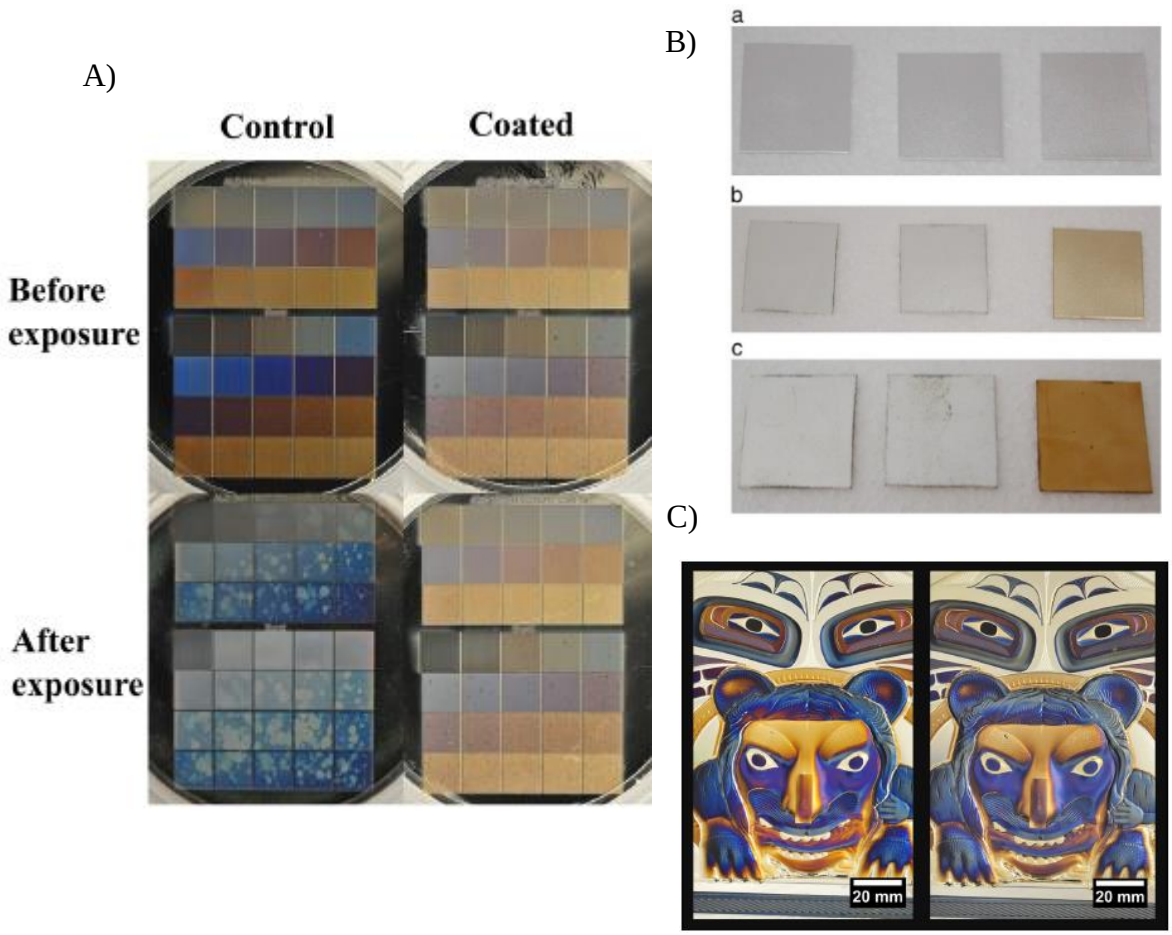

Figure 31. A) Effect of 15 nm Al_2O_3 ALD coating to the visual appearance of silver with plasmonic colors and effect of the ALD coating when samples are exposed to sulfur rich gas for 20 h.[148] Reprinted with permission from J.-M. Guay, G. Killaire, P. G. Gordon, S. T. Barry, P. Berini and A. Weck, *Langmuir*, 2018, **34**, 4998–5010. Copyright 2018 American Chemical Society. **B)** Tarnishing of ALD coated silver (left and middle) and silver with an organic protective layer (right), a before exposure, b after 5 h exposure and c after 48 h exposure to H_2S atmosphere.[146] Reprinted with permission from L. Paussa, L. Guzman, E. Marin, N. Isomäki and L. Fedrizzi, *Surface and Coatings Technology*, 2011, **206**, 976–980. Copyright 2011 Elsevier. **C)** Effect of 15 nm thick Al_2O_3 protective layer to the visual appearance of a silver object with plasmonic colors.[148] Reprinted with permission from J.-M. Guay, G. Killaire, P. G. Gordon, S. T. Barry, P. Berini and A. Weck, *Langmuir*, 2018, **34**, 4998–5010. Copyright 2018 American Chemical Society.

Corrosion of metal surfaces by ALD precursors is not discussed in literature, as the focus has been on corrosion by air and moisture. Apart from the exposure to the ALD precursors, the reactor chamber is vented to the atmospheric pressure when opened and thus it is exposed to oxygen and moisture. Corrosion of the metal parts due to exposure to the cleanroom air is however lowered by keeping the relative humidity in the cleanroom between approximately

40–50 %RH. Additionally, reactors are principally kept under vacuum and exposed to the cleanroom air only when opened, for example during maintenance or a batch change. Before opening the reactor, it is typically cooled down.

6.2 Barriers for preventing metal diffusion

As discussed in chapter "3.3.3 ALD in interconnects", atomic layer deposited diffusion barriers are used in copper interconnects to prevent diffusion of copper to the surrounding dielectric material as well as to prevent diffusion from the dielectric to the copper interconnects. Another application for ALD diffusion barriers is in lithium-ion batteries, where thin conformal barriers are needed to prevent diffusion of Li^+ ions from a lithium ion rich silicon to a silicon substrate.[56] Other applications for metal diffusion barriers deposited with ALD are found in solar energy harvesting technologies. Hafnium oxide has been used as a diffusion barrier between copper surface and solar absorbers[149] whereas aluminum oxide has been used to prevent metal diffusion from stainless steel substrate to the active $Cu(In,Ga)Se_2$ (CIGS) layer in thin-film solar cells.[150] Atomic layer deposited titanium oxide has been used to prevent diffusion from metal implants into body tissue.[151] Additionally, aluminum oxide can be used in TFEL displays to prevent the outdiffusion of sodium from soda lime glass, acting as the display substrate.[3]

Requirements for an effective barrier layer on a metal surface include good thermal and chemical stability, good adhesion, continuity and conformality, and proper microstructure.[152] Additional requirements depend on the application area of the barrier. For example, in the interconnect barriers conductivity, ability to enhance the subsequent copper deposition and suitability of the barrier deposition conditions to the IC manufacturing process must be considered.

One of the most important properties of a barrier film is microstructure. Possible microstructures of thin films are presented in Figure 32. Grain boundaries, especially when extending through the whole barrier film, provide an effective path for diffusion.[152] Therefore, polycrystalline and polycrystalline columnar structures are the most inconvenient for diffusion barriers. In practice, single crystal films would be ideal diffusion barriers, but deposition of conformal single crystal films is rarely possible. Therefore, nanocrystalline and amorphous film structures provide the best diffusion barriers.

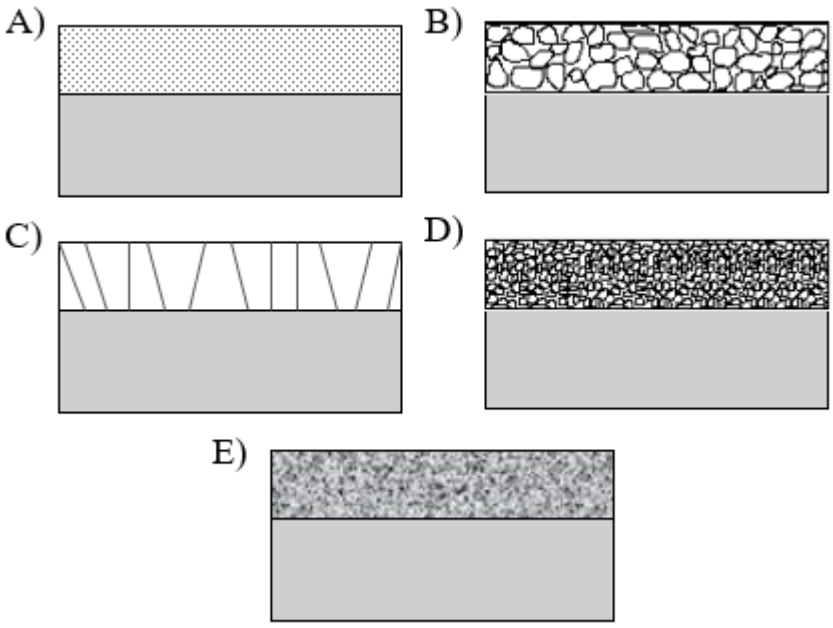

Figure 32. Possible thin film microstructures. **A)** Single crystal, **B)** Polycrystalline, **C)** Polycrystalline columnar, **D)** Nanocrystalline and **E)** Amorphous. According to Kaloyeros et al.[152]

Apart from a proper microstructure, diffusion barrier properties can be enhanced by utilizing layered structures i.e. nanolaminates. Nanolaminates are film stacks where typically two thin film materials are deposited alternately on top of each other. Thicknesses of the deposited material layers are in a nanometer scale. Strengths of nanolaminate structures in preventing metal impurity diffusion include nonequal diffusion coefficients of different metals in different film materials, and complicated diffusion paths for the impurities. As an example, if metal A diffuses fast in material 1 but slowly in material 2, and metal B does this vice versa, hindered diffusion of both metals can be obtained by applying a nanolaminate barrier consisting of the two materials. Formation of a complicated diffusion path is illustrated in Figure 33. If amorphous material layers are not used, the diffusion path complexity can be enhanced by keeping the layer thicknesses small and by selecting materials with mismatching lattice parameters, thus disturbing the grain growth.[153]

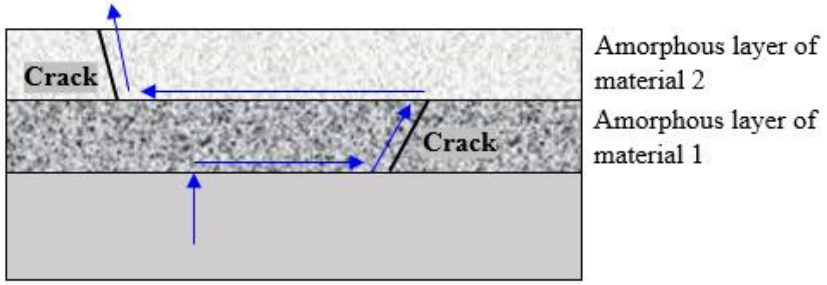

Figure 33. Illustration of an impurity diffusion path (blue arrows) through a double layer coating consisting of two amorphous materials.

When deposited from TMA and water, ALD aluminum oxide is amorphous at all applicable deposition temperatures up to 500 °C.[26] The almost ideal TMA/H_2O process and amorphous structure of films deposited even at high temperatures make aluminum oxide an attractive barrier material. Majumder et al.[59,154] presented the use of thin Al_2O_3 layers as copper diffusion barriers between copper and silicon. Copper diffusion was prevented with 2 nm thick Al_2O_3 film when the structure was exposed to temperatures below 700 °C in nitrogen atmosphere. With 1 nm thick barrier the failure temperature was 675 °C. Deposition of the barrier films was done with the $Al(NEt_2)_3/O_3$ ALD process at 250 °C and the films were amorphous. Bae et al.[150] presented the use of aluminum oxide as a metal diffusion barrier on stainless steel. Iron diffusion from stainless steel was found to reduce by 95 % with a 300 nm thick amorphous barrier layer deposited with the TMA/H_2O process.

Apart from Al_2O_3 Majumder et al.[59,154] presented the use of atomic layer deposited HfO_2 barriers to prevent copper diffusion. Failure temperatures were 675 and 650 °C for 2 and 1 nm thick HfO_2 barrier layers respectively. These non-crystalline hafnium oxide layers were deposited with the $Hf(NEt_2)_4/O_3$ ALD process at 250 °C. Thus, hafnium oxide barriers failed at 25 °C lower temperatures than the corresponding aluminum oxide films. Kotilainen et al.[149] presented HfO_2 diffusion barriers against copper, deposited from $Hf(NMe_2)_4$ and water at 200 °C. X-ray diffractograms of the films shoved amorphous structure. Hafnium oxide films were deposited on copper and their barrier efficiency was studied by annealing the samples in air at elevated temperatures. With a 49 nm thick barrier CuO hillock formation on the HfO_2 surface was detected at 400 °C due to copper diffusion through the barrier. At 300 °C no hillock formation was observed.

7. Summary

Semiconductor industry is a multibillion business, manufacturing products relevant to all consumers using electronic devices. One of the most important form of semiconductors is integrated circuits that are used in modern electronics and emerging technologies. The development and innovations in the field of electronics have made the formation of new generations, more efficient devices possible. Simultaneously the trends in the semiconductor industry have maintained the price development of these devices, manufactured with more and more novel methods, such that they are still available to common consumers with viable prices. For over four decades this development has been guided by the Moore's law.

The semiconductor downscaling has now reached the point where the continuum of Moore's law in its original form long to the future is not realistic. Downscaling alone is no longer efficient method for gaining more powerful devices due to the problems that have appeared such as heat generation and leakage currents. Device engineering together with new materials and deposition methods is needed. Atomic layer deposition is one of the most promising emerging technology candidates to be used in the field of microelectronics. In fact, ALD is already in commercial use in semiconductor industry, but most likely new ways for its utilization are yet to emerge. Academic literature on the use of ALD in the deposition of electrodes and dielectrics in DRAM capacitors, gates, gate dielectrics, spacers and channel / gate dielectric interfaces in MOSFETs and diffusion barriers, seed and adhesion layers in interconnects has been presented. The most frequently used ALD materials in these devices are metal oxides and metal nitrides.

Semiconductor devices can be severely damaged by contamination from the fabrication process. Metallic contamination is one of the most harmful forms of contamination in semiconductor manufacturing as it can harm the reliability, performance and yield of the devices. The atomic layer deposited materials used in microelectronics are deposited in an ALD reactor which is constructed of metal alloys, acting as possible contamination sources. Devices are vulnerable to metal contamination during the ALD processing steps, as the thicknesses of the deposited layers are in a nanometre regime and their integrity is in a key role for the proper functioning of the devices. Aggressive nature of the ALD precursors and the elevated temperatures used in the depositions increase the risk of metal impurity incorporation from the reactor to the devices.

Specifications for the tolerable metal contamination concentrations have been given e.g. by ITRS and IRDS. However, construction of a universal list of metals and their tolerable concentrations is not straightforward as these limits depend on the processing step as well as the processed devise. However, the trend of these specifications has been tightening, which further emphasises the importance of noncontaminating processing equipment. Extremely sensitive analysis methods are needed to monitor and control the metal concentrations in the processing line.

One method to reduce and control metal impurity concentrations transferred from the processing equipment to the samples is the application of protective coatings. Atomic layer deposited protective coatings have been used as corrosion and diffusion preventing layers. These materials consist mostly of metal oxides and metal nitrides. Advantages of ALD as a deposition method for protective layers include e.g. conformality and good quality of the deposited films. One important factor determining the effectiveness of a diffusion barrier is its microstructure. Especially amorphous films are potentially efficient diffusion barriers as they do not possess grain boundaries. ALD aluminum oxide is a well-known example of an amorphous material with a close to ideal deposition chemistry. Diffusion barrier properties can be further enhanced with the use of nanolaminates i.e. layered stack structures. Apart from the diffusion prevention, protection offered by the protective layer is determined by its reactivity with the gaseous precursors it is exposed to. As ALD offers the possibility to deposit over a hundred different materials, the reactivity between the protective layer and the precursors can be minimised by utilizing different coatings.

Based on the literature review conducted in this thesis, ALD has proved to be valuable method for semiconductor processing, and most likely its applications in that field will diversify in the future. However, the issue of the metal contamination risk in the ALD processing step must be considered and methods for its reliable control have to be developed. Based on this survey and the results presented in the academic literature on protective ALD coatings, atomic layer deposited thin films on reactor surfaces can be considered as a promising method for metal contamination control.

EXPERIMENTAL

8. Experimental methods

8.1 Introduction

Motivation for the experiments was **A)** to investigate if chosen ALD precursors etch metal components from metal surfaces and deliver them onto a silicon substrate through the gas phase, and **B)** to study if ALD coatings on top of the contamination source affect the level of metal contamination on the silicon wafer. In the experimental set-up the silicon substrate and the metal surface were not in contact, and thus the possible impurity transfer could occur only through the gas phase.

Those metal parts that belonged to the ALD reactor and were convenient to passivate, i.e. the reactor chamber and cassette, were coated with aluminum oxide prior to use. Contamination originating from the reactor itself was studied by measuring a background, which was extracted from the actual measurements. Separate, 200 mm circular metal plates were used as the metal contamination sources.

Three typical construction materials were studied as the contamination sources together with TMA and $CpHf(NMe_2)_3$ precursors as etching agents. Aluminum oxide, hafnium oxide and aluminum oxide – hafnium oxide nanolaminates were used as passivation layers. The metal contamination was measured from 200 mm silicon wafers. Experiments were conducted by exposing the contamination source and measurement wafer simultaneously to the ALD precursor inside an ALD reactor. During the experiments, it was important to minimize all contamination originating outside the experimental set-up, e.g. from handling and storing the wafers.

8.2 ALD reactor

All depositions and precursor exposures were carried out in a Beneq TFS 200 ALD reactor (Figure 34). The reactor was operated through the top lid, because a batch set-up was used. Reactor pressure during depositions and exposures was between 0.6–1.3 mbar. Nitrogen (99.9999 %, AGA) was used as a carrier and purging gas.

A) B)

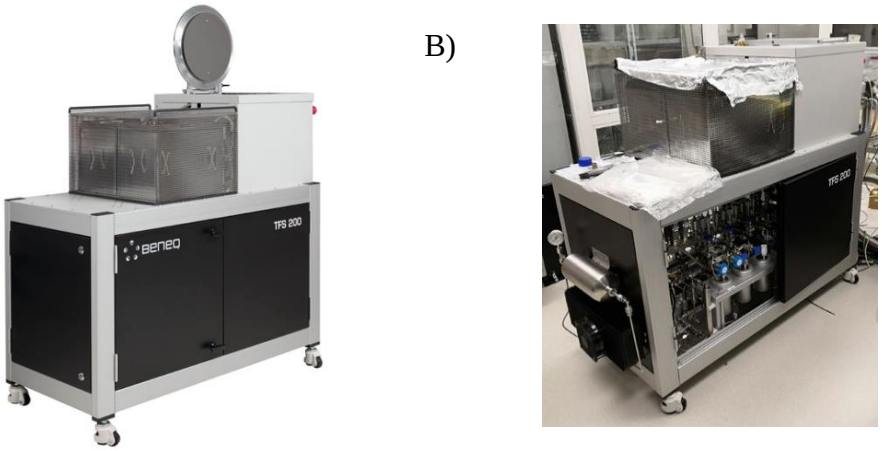

Figure 34. Beneq TFS 200 ALD reactor, **A)** marketing picture[155] and **B)** the reactor used in the experiments.

The reaction chamber is presented in Figures 35A and 35B. A ten-slot metal rack presented in Figure 35C was used as the cassette. The reactor chamber and cassette were both made from aluminum alloy. Before starting the exposure series these parts were sandblasted, washed and passivated with 750 nm aluminum oxide and 300 nm aluminum hafnium oxide for $CpHf(NMe_2)_3$ and TMA exposure series respectively. The TMA used for the passivation was electronic grade before the TMA exposure series and 98 % purity TMA from STREM chemicals before the $CpHf(NMe_2)_3$ exposure series due to practical reasons. The same sequential washing procedure was used with the chamber and cassette as with the metal plates (described in detail in section 8.3.2 Metal plates). Two different, but identical chamber cassette -pairs were used for the exposure series.

A B C

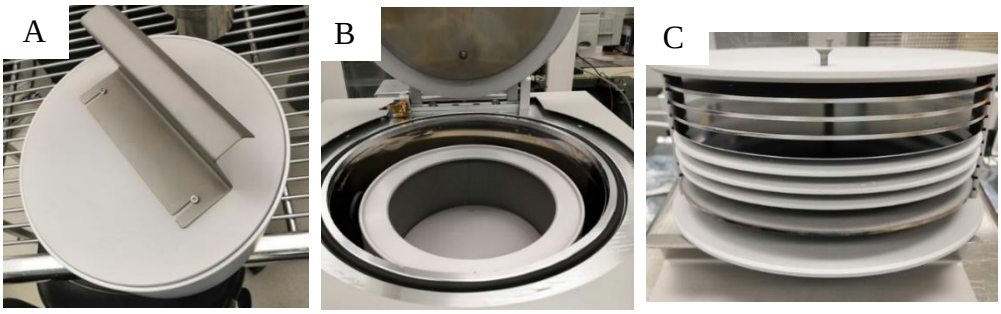

Figure 35. A) Reactor chamber with a lid and a lid lifter **B)** Reactor chamber inside the reactor **C)** Sample rack filled with metal plates going to passivation.

8.3 Method validation for a contamination study

8.3.1 Experimental set-up

200 mm p-type, boron doped, single side polished, <100> oriented silicon wafers were used as measurement wafers and dummies. The measurement wafer was placed in the cassette with the polished side towards the metal plate. The metal plates and the wafers were exposed to the studied precursors by pulsing the precursors into the chamber, one metal and one precursor at a time. Because only a single precursor was used, no film growth occurred. To avoid overloading the pump line, purging was done in between precursor pulses, and after the precursor pulsing one water pulse was given to neutralize the remaining precursor in the pump line. Thus, one ALD-cycle was grown on the wafers. To obtain uniform flow, the cassette was filled evenly with silicon wafers functioning as dummies. This set-up enabled metal transfer from the metal plate to the measurement silicon wafer through precursor interaction with the metal surface (Figure 36).

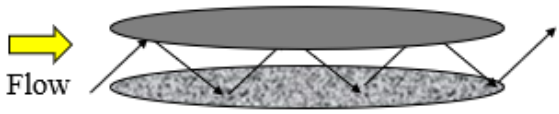

Figure 36. Interaction of gaseous precursor with the metal plate and silicon wafer.

The test set-up is presented in Figures 37A and 37B. The measurement wafer was positioned in slot 5, metal plate in slot 6 and the other slots were filled with dummies. In the first experiment, new dummy wafers were used, but they were not changed during the exposure series. In the background measurements the set-up was otherwise the same, but the metal plate was replaced with a silicon wafer. In the coating processes the cassette was filled with the metal plates to be coated, together with one silicon wafer for thickness measurement.

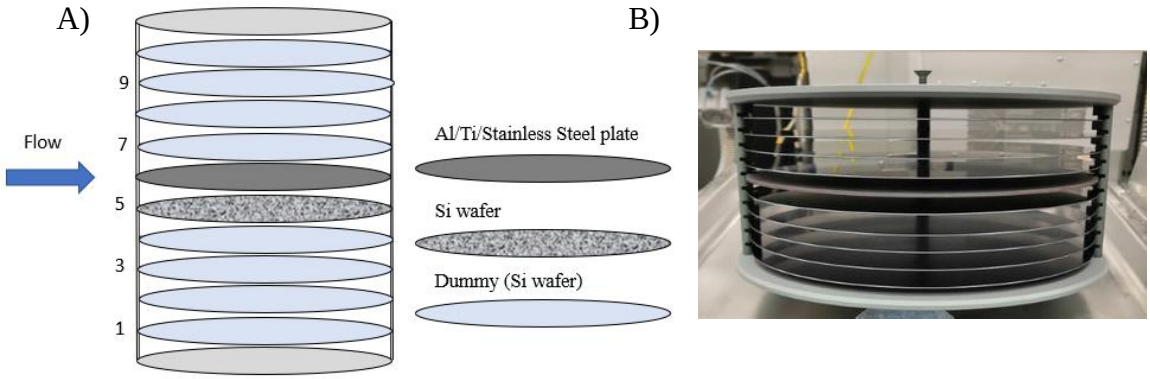

Figure 37. A) Schematic presentation and **B)** a photo of the sample set-up in the exposure tests. The silicon wafer for the ICP-MS measurement was placed in slot 5 and the metal plate in slot 6. Other slots were filled with dummies.

8.3.2 Metal plates

The metal parts studied were 200 mm plates made from aluminum 5754 (Al), grade 2 ASTM B265-15 titanium (Ti) and electropolished 316 stainless steel (SS). These materials were chosen based on their common use as construction materials. Stainless steel plates were polished because precursor delivery pipes are usually made from polished stainless steel. Benefits and drawbacks of the metals as construction materials are collected in Table 9. The major metal component is Al, Ti and Fe for aluminum, titanium and stainless steel respectively. Contents of different minor metal components in the aluminum, titanium and stainless steel plates are listed in Table 10. The composition information was gathered from the material certifications obtained from the suppliers. Apart from the listed metallic elements, the metals also contained carbon, silicon, nitrogen, sulfur, phosphorus, oxygen and hydrogen. Photos of the studied metal plates are presented in Figure 38.

Table 9. Benefits and drawbacks of aluminum, titanium and stainless steel as construction materials.

Metal	Benefit	Drawback
Aluminum	+ Light weight + Good heat conductivity + Easy to machine + Relatively low price	- Heat expansion - Easily corroded by chlorides
Titanium	+ No heat expansion + Inert towards chlorides	- High price - Difficult to machine
Stainless steel	+ Robust towards most chemicals + Easy to machine + Low price	- Heavy

Table 10. Minor metal components in the aluminum 5754 (Al), grade 2 titanium (Ti) and 316 stainless steel (SS) plates. Contents are given as weight percentages.

Metal (%)	Fe	Cu	Mn	Mn + Cr	Mg	Cr	Zn	Ti	Ni	Mo	Co
Al 5754	0.38	0.05	0.29	0.35	2.8	0.05	0.06	0.03			
Grade 2 Ti	0.07										
316 SS			1.33			16.56			10.01	2.02	0.228

A) B) C)

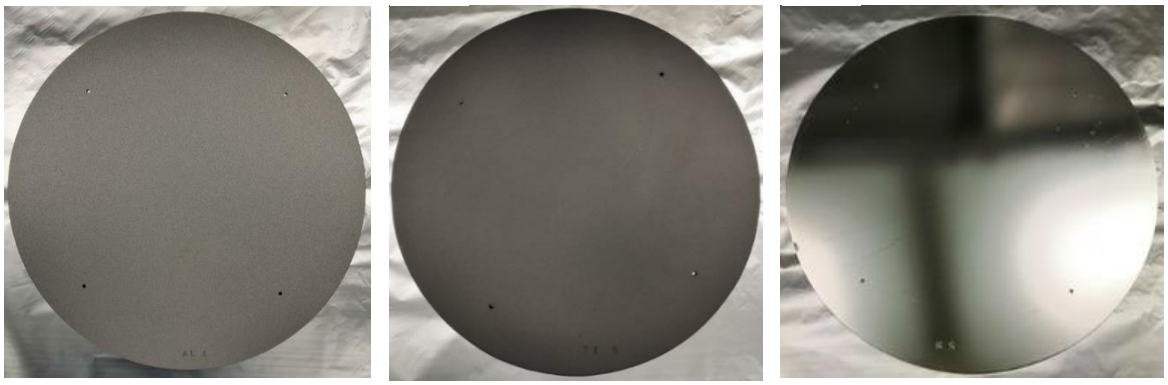

Figure 38. A) Aluminum **B)** Titanium and **C)** Electropolished Stainless steel plates used as contamination sources. Plates were photographed prior to depositions or exposures.

Identification marks were etched to the metal plates to ensure reliable identification of each plate. Titanium and aluminum metal parts were sandblasted with SiC prior to use. Fresh sand was used to lower the amount of contamination. Stainless steel parts were not sandblasted to maintain the polished surface. Metal plates were washed with tap water before and after the sand blasting.

After the transfer of the metal parts into a cleanroom, they were washed sequentially with hot tap water and isopropyl alcohol (isopropanol, IPA, approximately 25 w-% in de-ionized water) at least two times. After this, the parts were washed once with de-ionized water and once with the IPA-solution. All surfaces touching the metal plates during washing were covered with aluminum foil. The parts were dried after washing with a nitrogen jet and stored wrapped in aluminum foil and packed in vacuum bags. Handling and storing of the metal parts during and after the washing was done in a cleanroom.

8.3.3 Loading practice and handling of the wafers

Following a good loading practice, the cassette filling was done from the top to the bottom and unloading from the bottom to the top. When the exposure series was conducted, dummies were not moved but only the measurement silicon wafer and the metal plate were changed. The measurement wafers were obtained from a sealed wafer box dedicated to this project. The exposed wafers were packed and stored in a clean, new wafer box. The wafers were moved with a vacuum tweezer presented in Figure 39. The Teflon end of the tweezer was changed to a new one before the exposure series, and it was cleaned with isopropanol before and after each use and stored wrapped inside a cleanroom wipe. All handling of the wafers was done in a cleanroom with proper cleanroom equipment.

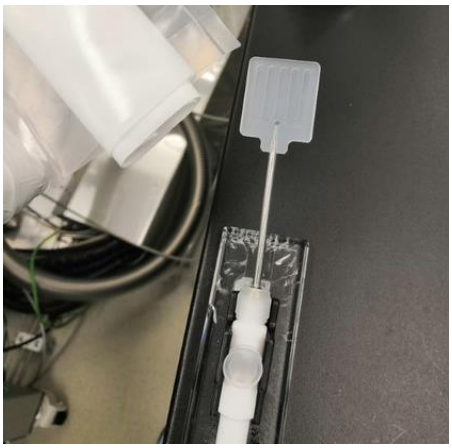

Figure 39. Vacuum tweezer with a changeable Teflon end used to move the silicon wafers.

8.3.4 Exposure of metals to ALD precursors

Two precursors were studied in the experiments, $CpHf(NMe_2)_3$ and electronic grade TMA (egTMA). egTMA was provided by Pegasus chemicals.[156] Electronic grade precursors were used to minimize the concentration of metal impurities originating from precursors themselves, see Tables 11 and 12 for the impurity consentrations of the precursors. Exposures of the metal plates to the precursors were carried out at 225 °C in all experiments.

Table 11. Impurity concentrations in the egTMA.

Concentration (ppm)	≤ 50	≤ 10	≤ 2	≤ 1	≤ 0.5	≤ 0.4	≤ 0.2	≤ 0.1	≤ 0.03	≤ 0.02
Elements	O	Cl	Si, S, I, Te, Sn, Pb	Sb, Se	Mo, As, Ni, Nb, Bi, Pd, P, Pt, Rh, Ge, Au, Tb, W, V, Hg	B, Cr, Co, Ag, La, Li	Co, Ti, Zn	Ba, Sr, Fe	Mn	Be, Cd, Mg, Y

Table 12. Impurity concentrations in the $CpHf(NMe_2)_3$.

Metal	**Concentration (ppb)**	**Metal**	**Concentration (ppb)**	**Metal**	**Concentration (ppb)**
Al	70	Pb	5	Th	5
Ba	5	Li	5	Sn	5
Ca	30	Mg	5	U	5
Cr	10	Mn	5	Zn	20
Co	5	Ni	5	Zr	120 000
Cu	5	K	5	Ti	100
Fe	20	Na	20		

The operation steps in the exposure test included loading of the cassette to the reactor, pump-down of the chamber, running (pre-heating and pulsing), venting of the reactor, and cooling of the cassette. The cassette was covered with a metallic lid during the cooling to avoid particles and air flows. The cooling time was 30 minutes. In the exposure tests the samples were not allowed to stand in the chamber after the pulsing, or in any other phase of the process, to minimize differences between the experiments.

8.4 Characterization

Film thicknesses, profiles and refractive indices of the passivation layers were measured from silicon with an ellipsometer. The 200 mm silicon wafers were mapped with a program using 69 measurement points with an exclusion area of 1 cm from the wafer edge. The used equipment was Sentech SE-400Adv with a measurement wavelength of 633 nm.

Metal contamination was analysed with ICP-MS from the 200 mm silicon wafers obtained from the exposure and background experiments. The ICP-MS measurements were carried out by Precilab, USA.[157] Total of 36 elements were analysed from the wafers: Al, Sb, As, Ba, Be, Bi, B, Cd, Ca, Cr, Co, Cu, Ga, Ge, Au, Fe, Pb, Li, Mg, Mn, Mo, Ni, Nb, Pt, K, Ag, Na, Sr, Ta, Tl, Sn, Ti, W, V, Zn and Zr. Two analysis equipment were used, Thermo Fisher Scientific XSeries II ICP-MS and Thermo Scientific iCAP Qs ICP-MS, former with the analysis of $CpHf(NMe_2)_3$ exposed samples and latter with the TMA exposed samples. Change in the analysis equipment was merely an equipment update carried out by Precilab. Used etchant for the sample preparation was 1.00 ml of 5 % HF / 2 % H_2O_2 water solution. The analysis covered the whole surface of the wafer. Li, Na, Mg, Al, K, Ca, Cr, Mn, Fe, Co, Ni and Cu were analysed using cool plasma with energy of 600 W and remaining elements using hot plasma with energy of 1550 W.

Additional X-ray diffraction (XRD) analysis were carried out from selected coatings. Analysis equipment was PANalytical X'Pert Pro MPD with CuKα radiation (1.5419 Å). The measurement was conducted with gracing incidence set-up using parallel beam optics with 1° fixed incident angle.

9. ALD passivation coatings

9.1 Aluminum oxide

Metal surface passivation was done with aluminum oxide using the TMA – water process. Two coating thicknesses were used, nominally 50 and 500 nm. The deposition temperature was 225 °C and the depositions were done in a Beneq TFS 200 ALD reactor. List of deposition parameters is presented in Table 13. The measured film thicknesses with their standard deviations and refractive indices measured from silicon wafers are presented in Table 14. Figure 40 presents film thickness mapping results for the nominal 50 nm film.

Table 13. Deposition parameters for the Al_2O_3-coatings on top of metal surfaces.

Target	Temperature (°C)	Pre-heat (h)	Precursors	Pulse sequence (s)	Cycles
Passivation 50 nm	225	3	TMA/H_2O	0.3/5 + 0.3/5	514
Passivation 500 nm	225	3	TMA/H_2O	0.3/5 + 0.3/5	5140

Table 14. Thicknesses with standard deviations, refractive indices and growth rates for Al_2O_3-coatings.

Film	Thickness (nm)	σ (nm)	n	GPC (nm/cycle)
Nominal 50 nm	58	0.442	1.647	0.113
Nominal 500 nm	568	2.436	1.650	0.110

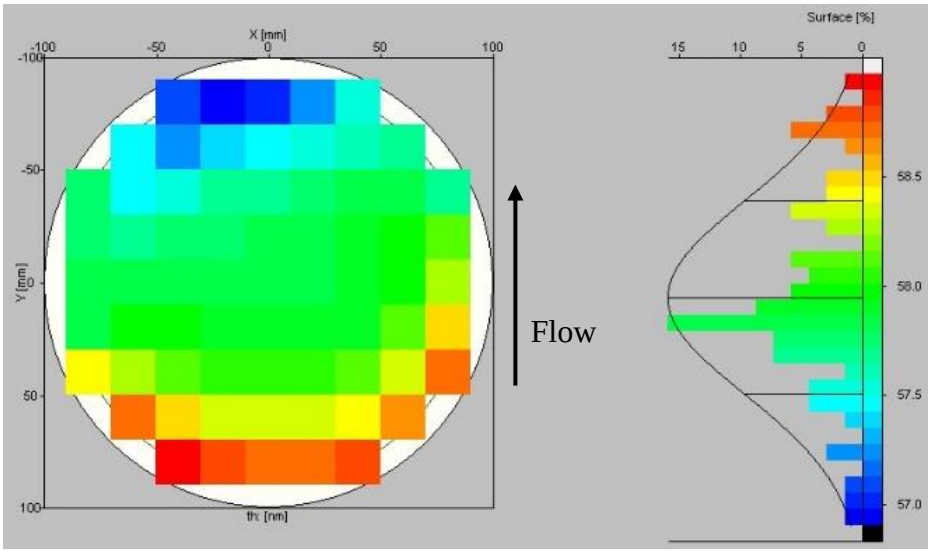

Figure 40. Thickness mapping of the nominal 50 nm Al_2O_3-film.

9.2 Hafnium oxide

$CpHf(NMe_2)_3$ – water process was used for the hafnium oxide deposition. The nominal film thickness was 50 nm. Table 15 shows the deposition parameters and Table 16 film characteristics. The hafnium pulsing was done with the load and release method described in detail in section 10.2. Thickness mapping of the HfO_2 film is presented in Figure 41. Literature values for HfO_2 growth rates are approximately 0.07 nm/cycle[69] with an ozone process at 225 °C and 0.023 nm/cycle[67] with water process at 305 °C.

Table 15. Deposition parameters for the HfO_2-coating on top of metal surfaces.

Target	Temperature (°C)	Pre-heat (h)	Precursors	Pulse sequence (s)	Cycles
Passivation 50 nm	225	3	$CpHf(NMe_2)_3/H_2O$	0.5/5.5 + 0.5/5	952

Table 16. Thickness with standard deviation, refractive index and growth rate for HfO_2-coating.

Film	Thickness (nm)	σ (nm)	n	GPC (nm/cycle)
HfO_2	45	0.976	2.037	0.0472

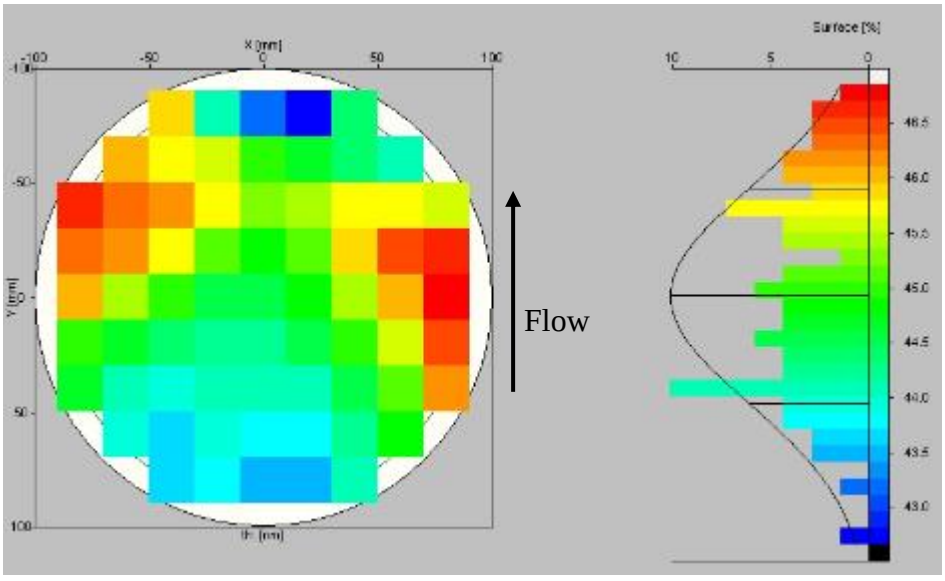

Figure 41. Thickness mapping of the nominal 50 nm HfO_2-film.

9.3 Aluminum oxide – hafnium oxide nanolaminate

Al_2O_3/HfO_2-nanolaminate was constructed as a 5 + 5 nm stack, with the nominal total thickness of the film being 50 nm. Deposition parameters are presented in Table 17, ellipsometer results in Table 18 and thickness mapping in Figure 42.

Table 17. Deposition parameters for the Al_2O_3/HfO_2-laminate on top of metal surfaces.

Target	Temperature (°C)	Pre-heat (h)	Precursors	Pulse sequence (s)	Cycles
Passivation 50 nm (5 + 5 nm stack)	225	3	egTMA/ H_2O $CpHf(NMe_2)_3/H_2O$	0.3/5 + 0.3/5 0.5/5.5 + 0.5/5	5 x (45 + 95)

Table 18. Thickness with standard deviation and refractive index for Al_2O_3/HfO_2 laminate.

Film	Thickness (nm)	σ (nm)	Refractive index
Al_2O_3/HfO_2-laminate	44	0.496	1.848

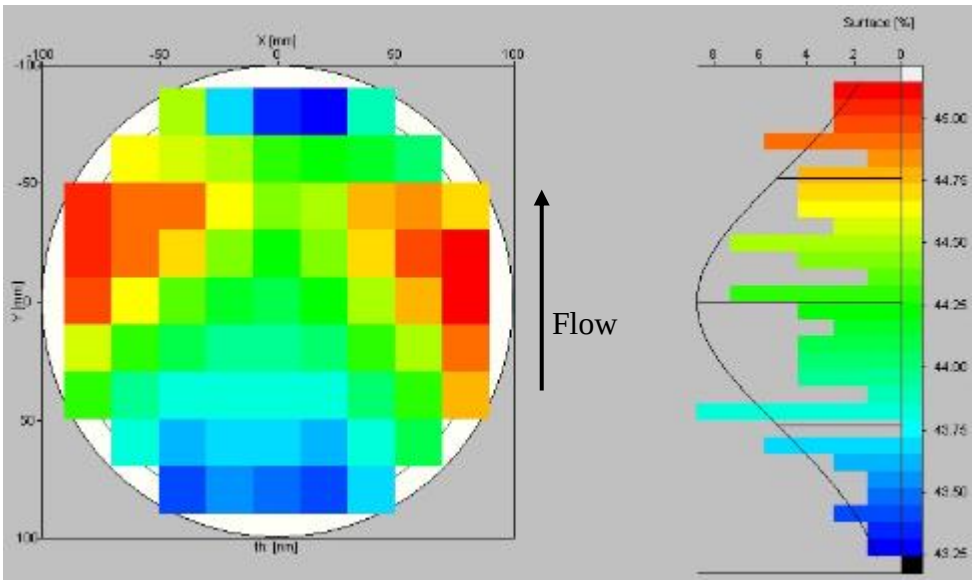

Figure 42. Thickness mapping of the nominal 50 nm Al_2O_3/HfO_2-laminate.

10. $CpHf(NMe_2)_3$ exposures with Al_2O_3 coatings

10.1 Background

Background was measured before and after the exposure experiments to examine the metal impurity level originating from the reactor without external metal pieces. This was done by placing a new silicon wafer into the reaction chamber and leaving it in vacuum for a time corresponding to an exposure experiment. No pulsing was conducted in the background experiments. Results from the backgrounds measured before (background 1, BG1) and after (background 2, BG2) the $CpHf(NMe_2)_3$ exposure experiments are presented in Figure 43.

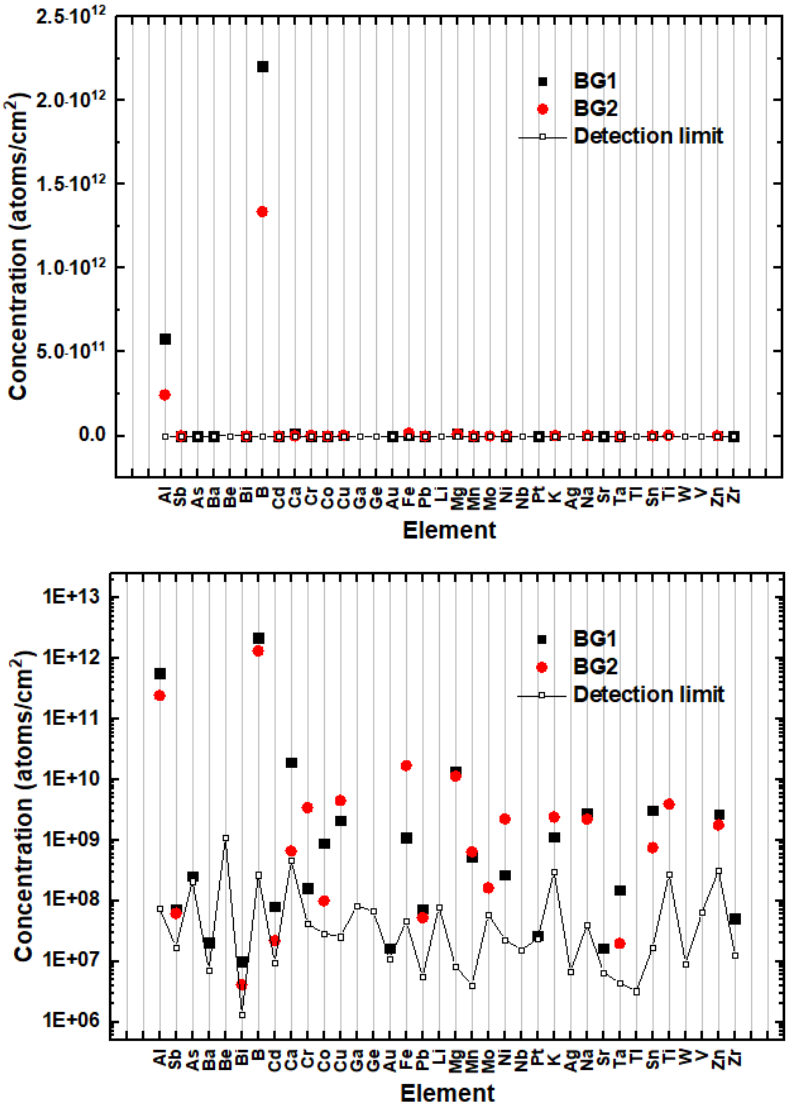

Figure 43. Background before (BG1) and after (BG2) running the $CpHf(NMe_2)_3$ exposure series on linear (top) and logarithmic (bottom) scale.

Aluminum and boron were present in clearly higher concentrations than the other elements measured (> $6 \cdot 10^{10}$ atoms/cm^2). Aluminum originates from the aluminum oxide passivated chamber and cassette, and boron is the dopant of the silicon wafers. Concentration ranges for the elements are summarized in Table 19.

Table 19. Concentration ranges of the elements present in the background experiments. The values are shown as averages from the two background experiments.

Concentration (atoms/cm^2)	**Element**
$1–9 \cdot 10^{12}$	B
$1–9 \cdot 10^{11}$	Al
$1–9 \cdot 10^{10}$	Ca, Mg
$1–9 \cdot 10^{9}$	Cr, Cu, Fe, Ni, K, Na, Sn, Ti, Zn
$1–9 \cdot 10^{8}$	As, Co, Mn, Mo
$1–9 \cdot 10^{7}$	Sb, Ba, Cd, Au, Pb, Pt, Sr, Ta, Zr
$1–9 \cdot 10^{6}$	Bi
Below detection limit	Be, Ga, Ge, Li, Nb, Ag, Tl, W, V

10.2 Exposure experiments

Due to the low vapour pressure of $CpHf(NMe_2)_3$, a hot precursor source at 120 °C was used together with the load and release method for the precursor pulsing. A schematic presentation of the load and release method with the pulse sequence used is presented in Figure 44. Valves 1, 2 and 3 were opened in sequence, first to fill the precursor source with nitrogen and then to deliver the $CpHf(NMe_2)_3$ pulse with the aid of overpressure to the reaction chamber. A detailed list of test parameters for the $CpHf(NMe_2)_3$ exposure experiments is collected in Table 20.

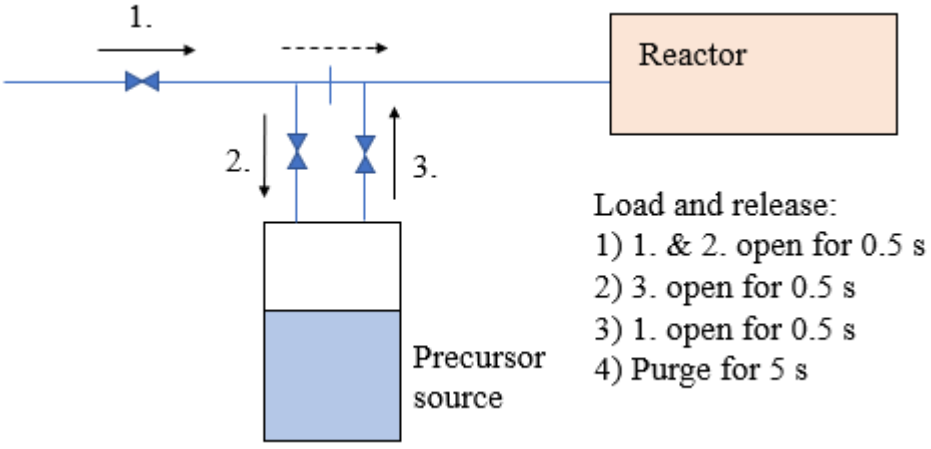

Figure 44. Schematic presentation of the load and release precursor pulsing.

Table 20. Parameters of metal – $CpHf(NMe_2)_3$ exposure tests.

Exposure precursor	Exposed metal	Temp. (°C)	Pre-heat (h)	Pulse (s)	Cycles
$CpHf(NMe_2)_3$	570 nm Al_2O_3 on Al	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	570 nm Al_2O_3 on Ti	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	570 nm Al_2O_3 on SS	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	59 nm Al_2O_3 on Al	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	59 nm Al_2O_3 on Ti	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	59 nm Al_2O_3 on SS	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	Bare Al	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	Bare Ti	225	3	0.5/0.5/0.5/5	500
$CpHf(NMe_2)_3$	Bare SS	225	3	0.5/0.5/0.5/5	500

Metal contamination results from the experiments with aluminum, titanium and stainless steel plates exposed to $CpHf(NMe_2)_3$ are presented in Figures 45–47 respectively. Average concentrations of the background experiments are deducted from the results and the metal components present in the exposed plates are marked with red. Thus, a missing data point means that the element was not detected at a level higher than in the background.

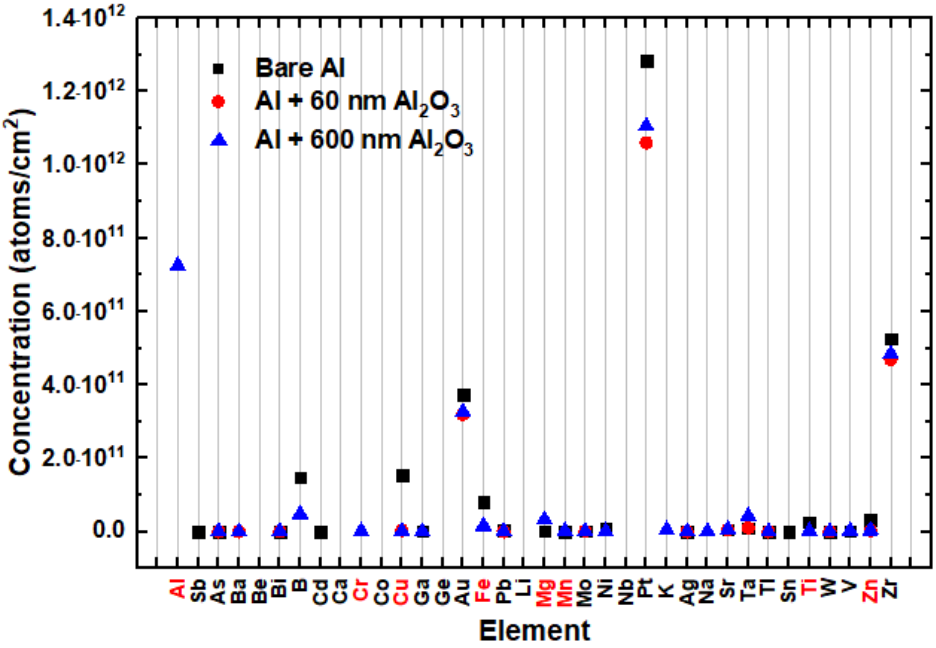

Figure 45. Metal contamination originating from aluminum plates without coating and with 60 and 600 nm Al_2O_3 coatings when exposed to $CpHf(NMe_2)_3$.

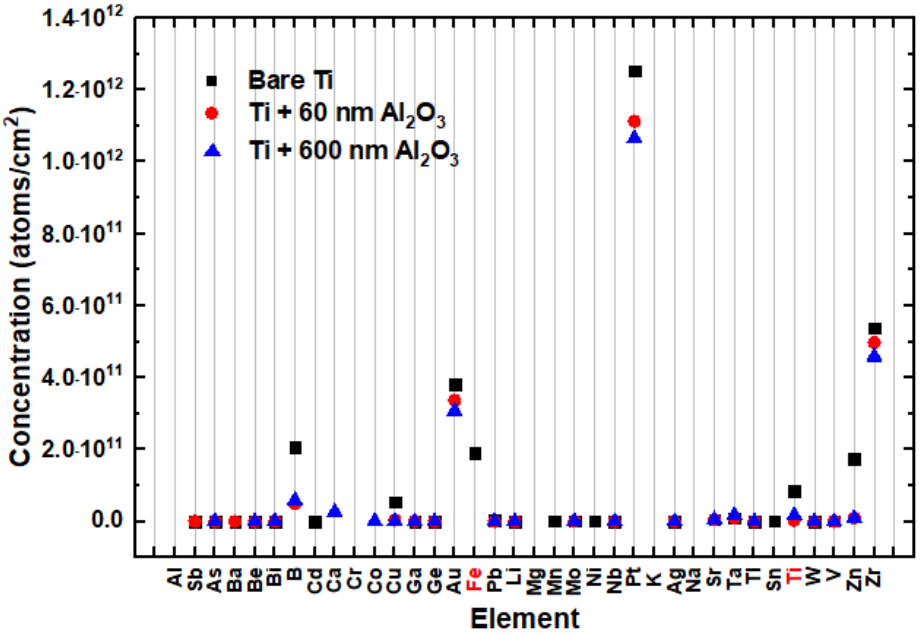

Figure 46. Metal contamination originating from titanium plates without coating and with 60 and 600 nm Al_2O_3 coated plates when exposed to $CpHf(NMe_2)_3$.

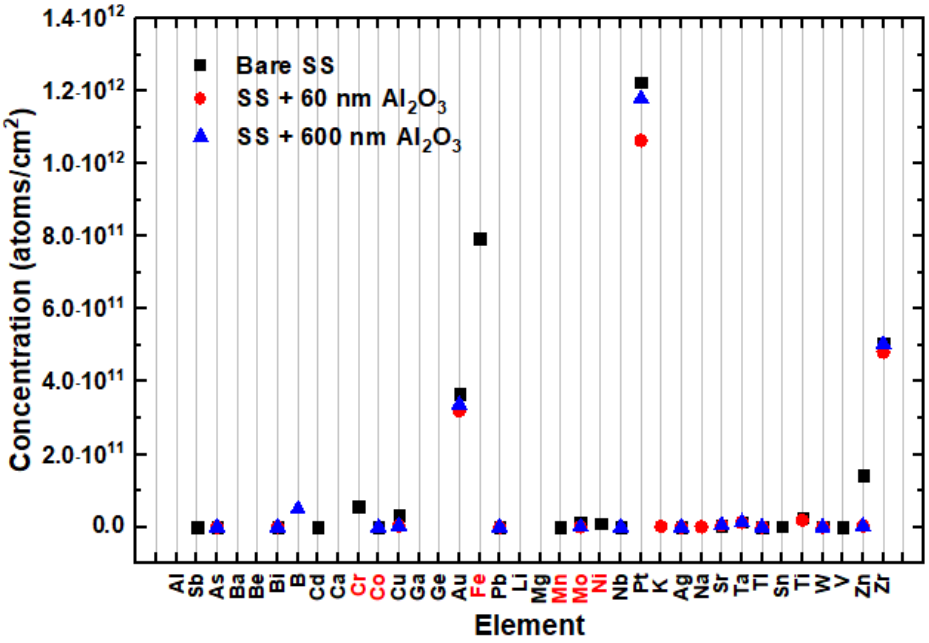

Figure 47. Metal contamination originating from stainless steel plates without coating and with 60 and 600 nm Al_2O_3 coated plates when exposed to $CpHf(NMe_2)_3$.

As can be seen from Figures 45–47, the metal impurity levels were systematically higher when the exposures were done with uncoated metal plates. Differences between 60 and 600 nm Al_2O_3 coated plates were rather small, and some metal concentrations were higher when the thicker aluminum oxide coating was applied. The elements not present in the metal plates that were detected in high concentrations compared to the others included Al, B, Au, Pt and Zr. Apart from aluminum, these metals were present in all measurements.

As already mentioned, boron is the silicon dopant and thus present in all measurements, and aluminum originates from the passivation coatings on the reactor parts and metal plates. Zirconium is the main impurity in $CpHf(NMe_2)_3$ and thus originates from the precursor. The reason for this is the similar chemistries of zirconium and hafnium. As both are group four elements in the periodic table, they have similar size and they appear together in the nature, which makes their efficient separation challenging.

The presence of gold and platinum is related to the history of the reactor. Both elements were systematically present on all the exposed wafers but not on the backgrounds, which implies that they did not originate from the wafer handling procedure, reaction chamber or cassette. These impurities could not originate from sandblasting either as stainless steel plates were not sandblasted but contained these impurities. Au and Pt are not $CpHf(NMe_2)_3$ impurities either according to the precursor certificate provided by the producer. These impurities must originate from the precursor line as they were present in all cases where pulsing was conducted and absent when not. For platinum this is logical as platinum containing films have been deposited in the reactor, and platinum has been pulsed from the same hot source as $CpHf(NMe_2)_3$. Gold most likely originates from gold containing samples that have been coated in the reactor. Regarding gold, it's absence from the background experiments and presence in the exposure experiments is interesting. This implies either that gold residues have invested into the hot source precursor line or that nitrogen alone is not able to transfer gold residues e.g. from the chamber walls to the measurement silicon wafer, and this occurs only with the $CpHf(NMe_2)_3$ pulsing.

One alternative source for the Au and Pt contamination is the Al_2O_3-barrier itself. If the barrier was contaminated with the metals because of the used TMA deposition precursor, these impurities could transfer from the barrier to the measurement silicon during the exposure. As the Au and Pt impurities were present after the exposures with the bare metal plates as well, the impurity transformation would occur also from the Al_2O_3 passivated reactor chamber.

11. TMA exposures with HfO_2 and Al_2O_3/HfO_2-nanolaminate coatings

11.1 Background

Background was measured before (background 1, BG1) and after (background 2, BG2) the TMA exposures, similarly as with $CpHf(NMe_2)_3$ exposures. Results from the background exposures are presented in Figure 48. Al and B were present in high concentrations due to the Al_2O_3 passivated chamber and cassette, and boron doped silicon wafers.

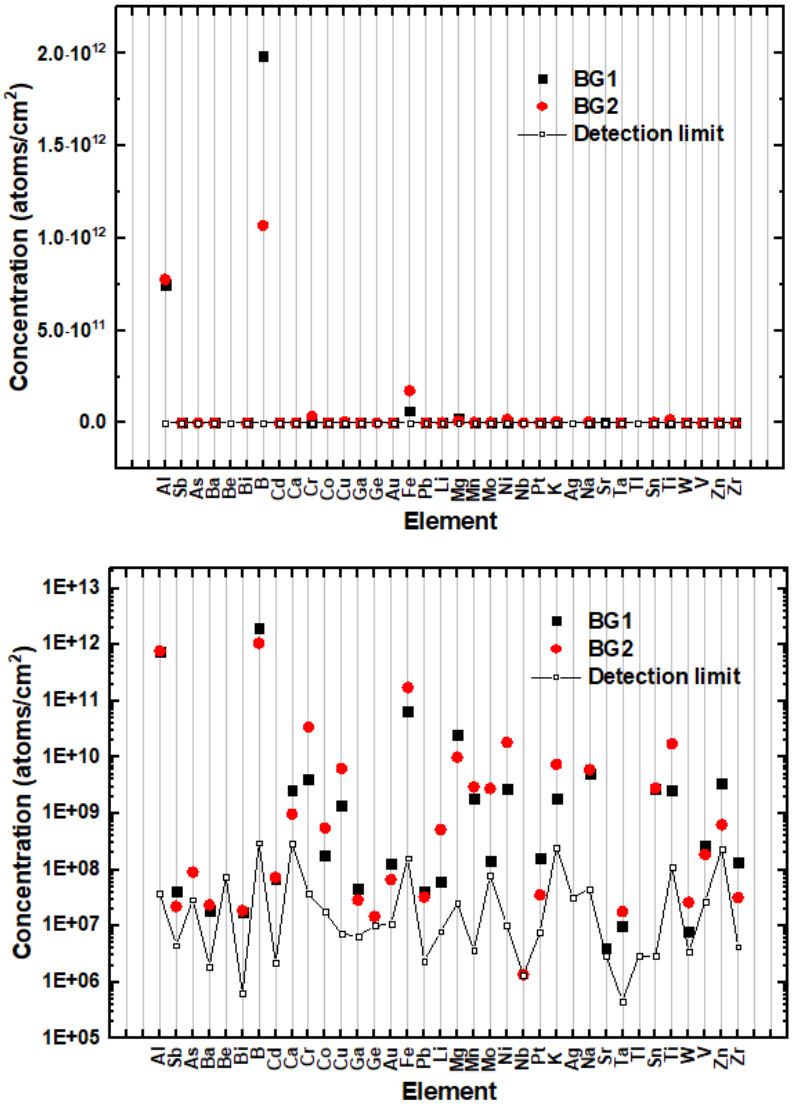

Figure 48. Background before (BG1) and after (BG2) running the egTMA exposure series on linear scale (up) and logarithmic scale (down).

As can be seen from Figure 48, chromium, iron and magnesium were present in slightly higher concentrations than the other elements, which refers to residues from unpassivated aluminum. In BG1 these residues originate from the aluminum chamber, whose bottom was not completely covered with aluminum oxide because the cassette and the chamber were passivated simultaneously. In BG2 the increase in metal impurities originates from the TMA exposed uncoated metal plates. Elements are grouped based on their concentrations in Table 21.

Table 21. Concentration range of the elements present in the background. The values are shown as averages from the two background experiments. Results from the $CpHf(NMe_2)_3$ exposures are shown for reference.

Concentration (atoms/cm^2)	**Element, TMA exposures**	**Element, $CpHf(NMe_2)_3$ exposures**
$1–9 \cdot 10^{12}$	B	B
$1–9 \cdot 10^{11}$	Al, Fe	Al
$1–9 \cdot 10^{10}$	Cr, Mg, Ni, Ti	Ca, Mg
$1–9 \cdot 10^{9}$	Ca, Cu, Mn, Mo, K, Na, Sn, Zn	Cr, Cu, Fe, Ni, K, Na, Sn, Ti, Zn
$1–9 \cdot 10^{8}$	Co, Li, V	As, Co, Mn, Mo
$1–9 \cdot 10^{7}$	Sb, As, Ba, Bi, Cd, Ga, Ge, Au, Pb, Pt, Ta, W, Zr	Sb, Ba, Cd, Au, Pb, Pt, Sr, Ta, Zr
$1–9 \cdot 10^{6}$	Nb, Sr	Bi
Below the detection limit	Be, Ag, Tl	Be, Ga, Ge, Li, Nb, Ag, Tl, W, V

11.2 Exposure experiments

Test parameters for egTMA exposure experiments are collected in Table 22. Other parameters were the same as in the $CpHf(NMe_2)_3$ exposures, but pulsing was changed to represent a typical TMA pulsing, the load and release method was not required.

Table 22. Parameters for the metal – egTMA exposure tests.

Exposure precursor	Exposed metal	Temperature (°C)	Pre-heat (h)	Pulse (s/s)	Cycles
TMA	44 nm Al_2O_3/HfO_2 on Ti	225	3	0.3/5	500
TMA	44 nm Al_2O_3/HfO_2 on Al	225	3	0.3/5	500
TMA	44 nm Al_2O_3/HfO_2 on SS	225	3	0.3/5	500
TMA	45 nm HfO_2 on Ti	225	3	0.3/5	500
TMA	45 nm HfO_2 on Al	225	3	0.3/5	500
TMA	45 nm HfO_2 on SS	225	3	0.3/5	500
TMA	Bare Ti	225	3	0.3/5	500
TMA	Bare Al	225	3	0.3/5	500
TMA	Bare SS	225	3	0.3/5	500

Contamination levels originating from the tests with uncoated, 45 nm HfO_2 and 44 nm Al_2O_3/HfO_2-laminate coated metal plates exposed to TMA are presented in Figures 49–51. Again, the average concentrations of the background tests are deducted from the results and the metal components present in the exposed plates are marked with red. Aluminum was excluded from the results due to its high concentration originating from the TMA precursor. The aluminum concentration in the backgrounds was $8 \cdot 10^{11}$ atoms/cm^2 and $7 \cdot 10^{11}$ atoms/cm^2 for the first and second background measurements respectively. In the exposure series the aluminum concentartion varied between 4–$7 \cdot 10^{14}$ atoms/cm^2. Thus, the precursor exposure and the grown one ALD-cycle of Al_2O_3 increased the aluminum concentration with approximately three orders of magnitude.

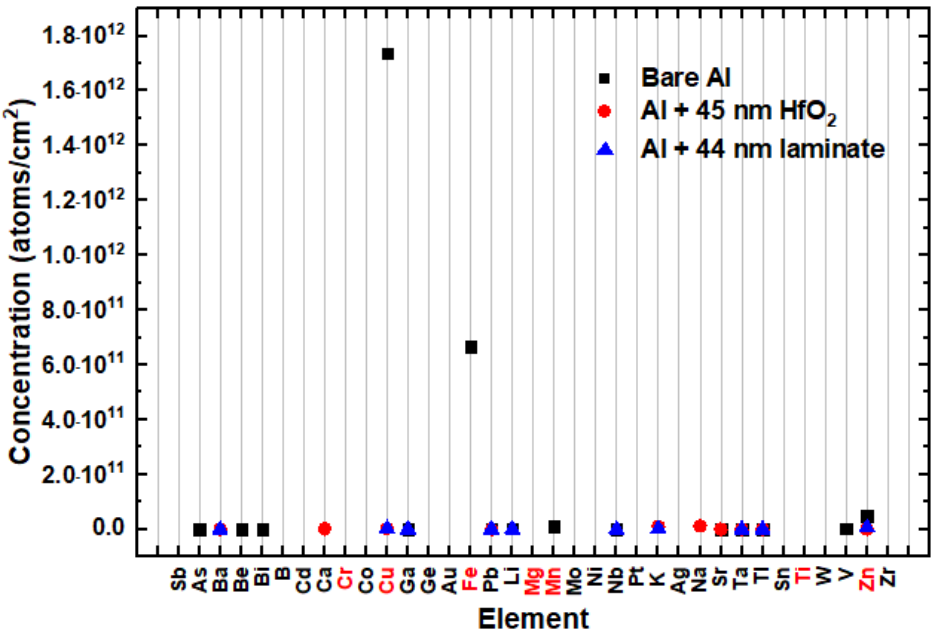

Figure 49. Metal contamination originating from aluminum plates without coating and with 45 nm HfO_2 and 44 nm HfO_2/Al_2O_3-laminate coatings when exposed to TMA.

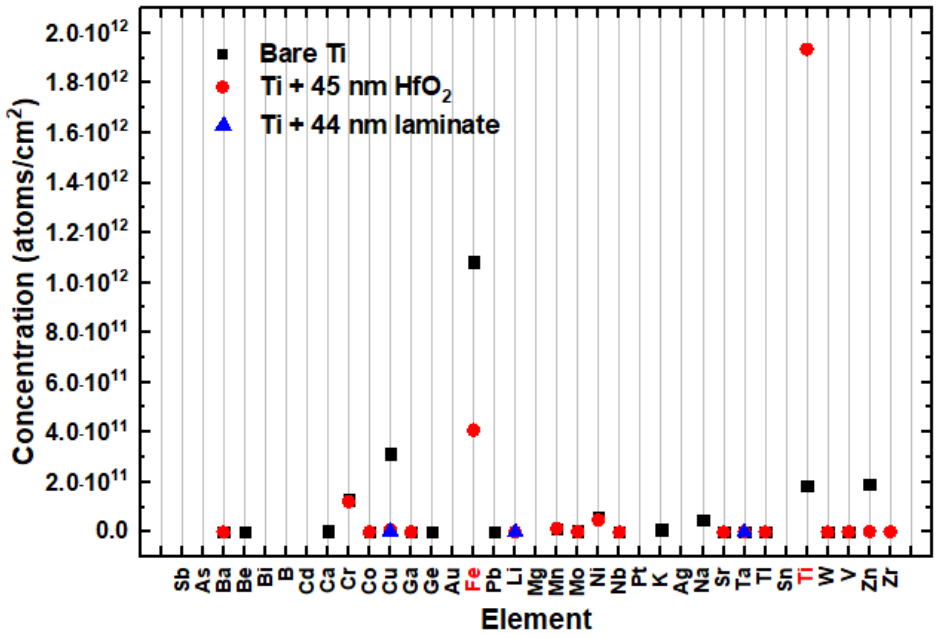

Figure 50. Metal contamination originating from titanium plates without coating and with 45 nm HfO_2 and 44 nm HfO_2/Al_2O_3-laminate coatings when exposed to TMA.

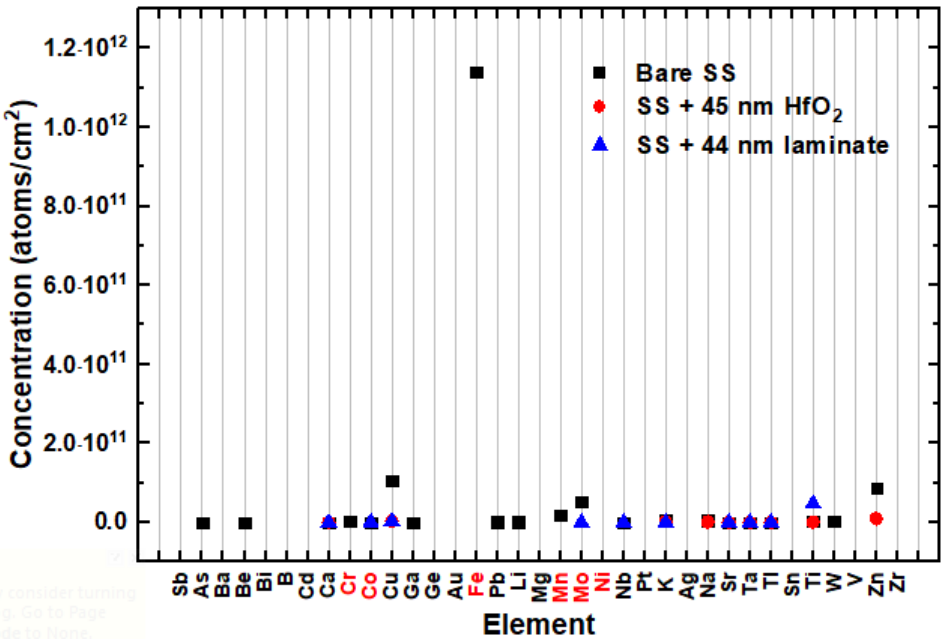

Figure 51. Metal contamination originating from stainless steel plates without coating and with 45 nm HfO_2 and 44 nm HfO_2/Al_2O_3-laminate coatings when exposed to TMA.

Similar to the aluminum oxide coatings, the hafnium oxide and nanolaminate coatings lowered the metal impurity concentrations. This time no high Au, Pt or Zr concentrations were detected. This supports the assumption that Au and Pt impurities originated from the hot source or the related precursor line, or from the Al_2O_3-barriers on the reactor chamber and the metal plates. A room temperature source with a different precursor line was used with TMA and this time the passivation of the chamber was done with egTMA instead of the 98 % purity TMA. Zr was not detected because TMA was used as the exposure precursor instead of $CpHf(NMe_2)_3$.

With the titanium plates the titanium concentration was higher with the hafnium oxide coated plate than with the uncoated titanium plate, which refers to poor passivation properties of hafnium oxide on titanium or to a contaminated sample. High iron concentration with all unpassivated metal plates and high copper concentration with the unpassivated aluminum plate originate from the metal plates. With the coated metal plates the corresponding metal concentrations are significantly lower. This effectively demonstrates the role of the passivation coatings: passivation of the metal plate with an ALD coating hinders or prevents the transportation of the metallic species into the silicon wafer.

12. Comparison of the barrier coatings

Contamination levels from aluminum, titanium and stainless steel plates without coating and with 60 nm Al_2O_3, 600 nm Al_2O_3, 45 nm HfO_2 and 44 nm Al_2O_3/HfO_2-laminate coatings exposed to $CpHf(NMe_2)_3$ or TMA are presented respectively in Tables 23–25 and in the corresponding Figures 52–54. From all the measured elements, only those present as major or minor components in the metal plates in question are presented. However, with aluminum plates aluminum is excluded as it can originate from TMA and Al_2O_3 passivated chamber parts.

Table 23. Impurity concentrations from aluminum plates with different coatings. Numbers in the brackets are the contents of the metal components in aluminum as wt. %. Blue shading refers to exposure to $CpHf(NMe_2)_3$) and yellow to TMA. BDL = below detection limit.

Coating	Mg (2.8)	Fe (0.38)	Mn (0.29)	Zn (0.06)	Cu (0.05)	Cr (0.05)	Ti (0.03)
Bare	3E+09	8E+10	3E+08	3E+10	2E+11	BDL	3E+10
60 nm Al_2O_3	BDL	BDL	BDL	2E+09	3E+09	BDL	BDL
600 nm Al_2O_3	3E+10	2E+10	2E+09	3E+09	1E+09	9E+08	2E+09
Bare	BDL	7E+11	1E+10	5E+10	2E+12	BDL	BDL
45 nm HfO_2	BDL	BDL	BDL	5E+08	3E+09	BDL	BDL
44 nm laminate	BDL	BDL	BDL	6E+09	3E+09	BDL	BDL
Detection limit	8E+06	5E+07	4E+06	3E+08	3E+07	4E+07	3E+08

Table 24. Impurity concentrations from titanium plates with different coatings. Numbers in the brackets are the contents of the metal components in titanium as wt. %. Blue shading refers to exposure to $CpHf(NMe_2)_3$) and yellow to TMA. BDL = below detection limit.

Coating	Ti (major)	Fe (0.07)
Bare	8E+10	2E+11
60 nm Al_2O_3	3E+09	BDL
600 nm Al_2O_3	2E+10	BDL
Bare	2E+11	1E+12
45 nm HfO_2	2E+12	4E+11
44 nm laminate	BDL	BDL
Detection limit	3E+08	5E+07

Table 25. Impurity concentrations from stainless steel plates with different coatings. Numbers in the brackets are the contents of the metal components in stainless steel as wt. %. Blue shading refers to exposure to $CpHf(NMe_2)_3$) and yellow to TMA. BDL = below detection limit.

Coating	Fe (major)	Cr (16.56)	Ni (10.01)	Mn (1.33)	Mo (2.02)	Co (0.228)
Bare	8E+11	6E+10	1E+10	3E+08	2E+10	3E+08
60 nm Al_2O_3	BDL	BDL	BDL	BDL	6E+08	BDL
600 nm Al_2O_3	BDL	BDL	BDL	BDL	8E+08	2E+07
Bare	1E+12	3E+09	BDL	2E+10	5E+10	BDL
45 nm HfO_2	BDL	BDL	BDL	BDL	BDL	BDL
44 nm laminate	BDL	BDL	BDL	BDL	6E+06	BDL
Detection limit	5E+07	4E+07	2E+07	4E+06	6E+07	3E+07

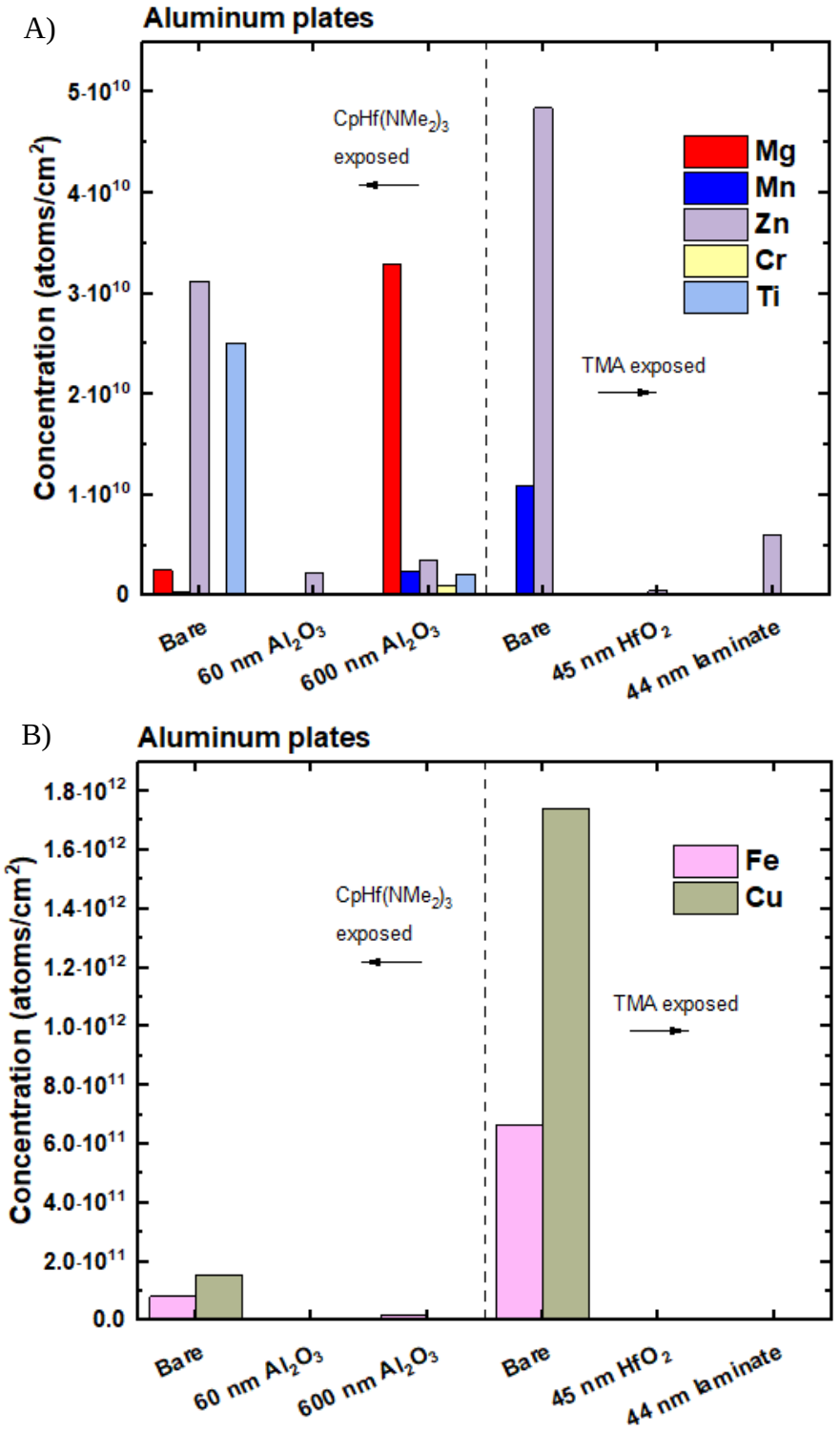

Figure 52. Metal impurities originating from aluminum plates without and with different passivation coatings. **A)** Mg, Mn, Zr, Cr, Ti impurities, **B)** Fe and Cu impurities.

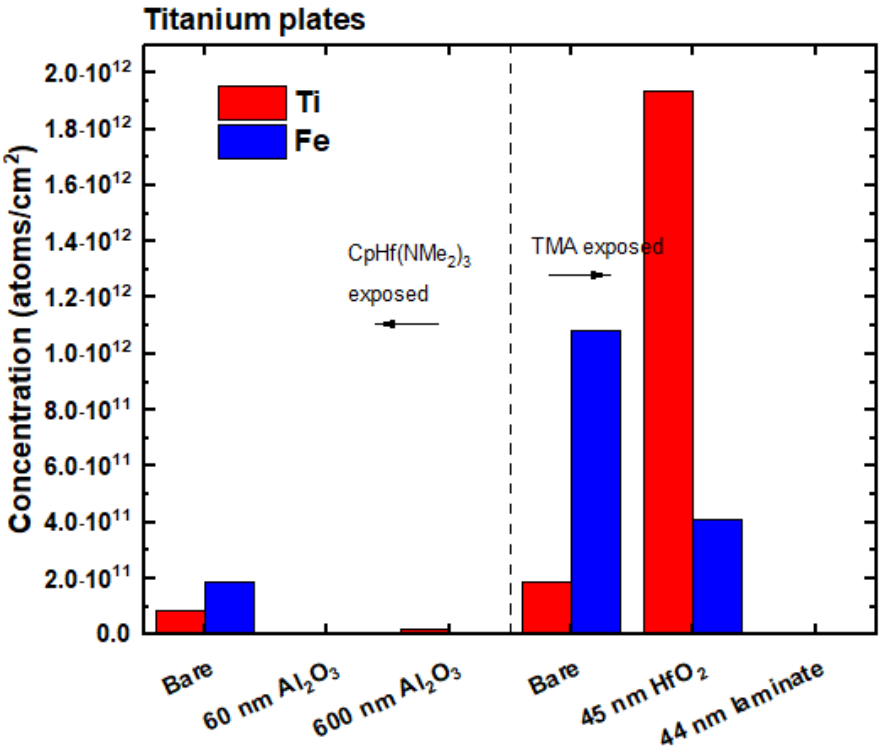

Figure 53. Metal impurities originating from titanium plates without and with different passivation coatings.

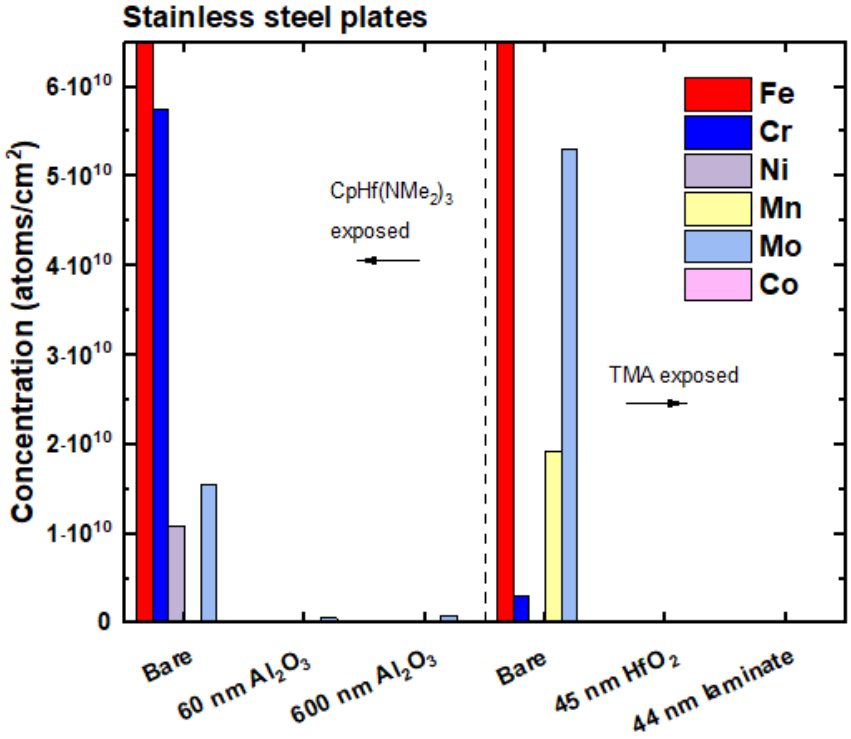

Figure 54. Metal impurities originating from stainless steel plates without and with different passivation coatings.

With aluminum plates the decrease in metal impurities due to the coatings was evident especially with iron and copper. Cu and Fe were detected in higher concentrations when bare plates were exposed to TMA than when exposed to $CpHf(NMe_2)_3$, which implies more aggressive reactions between TMA and the metal than with $CpHf(NMe_2)_3$ and the metal. With 600 nm Al_2O_3 passivated plate, concentrations for Mg, Mn, Cr, Zn and Ti were rather high. Zn was present in all samples. Magnesium most likely originates from the operator. This is supported by the increased concentrations of Na ($9.8 \cdot 10^7$ atoms/cm^2) and K ($5.1 \cdot 10^9$ atoms/cm^2) from the 600 nm Al_2O_3 passivated plate, with both Na and K being absent in samples made with the uncoated and 60 nm Al_2O_3 passivated plates. Zn, Mn and Cr most likely originate from the cleanroom air, as display production is conducted in the same cleanroom. ZnS:Mn is utilized as the phosphor layer and Cr in the electrodes of the electroluminescent displays.

The only metals originating from the titanium plates were titanium and iron. Even though iron is a minor component in the titanium plates, it was detected in higher concentrations than titanium. This supports the consideration of iron as a readily moving metal impurity, as discussed in the literature part of this thesis. Similarly as with the aluminum plates, TMA seems to etch the uncoated metal plate more aggressively than $CpHf(NMe_2)_3$ as both titanium and iron concentrations were higher when titanium was exposed to TMA. Aluminum oxide and nanolaminate coatings were efficient against metal impurity transfer onto the silicon wafer. However, with the HfO_2 passivation higher impurity levels for both metals were detected than with the uncoated plates. This implies that HfO_2 does not provide efficient passivation for titanium or that the sample was contaminated. XRD-measurements from the HfO_2 films were conducted to see if the films were crystalline, which could explain the poor diffusion barrier properties. However, the measurement results did not suggest the film to be crystalline.

With stainless steel plates the passivation was very successful. Only molybdenum and cobalt were detected from the exposure experiments with the coated plates, whereas iron, chromium, nickel and manganese were all absent. Especially the iron concentration was significantly decreased with all the coatings. With the uncoated stainless steel plates, the impurity concentrations of some metals were higher when exposed to TMA and with others when exposed to $CpHf(NMe_2)_3$.

To compare the efficiency of the different coatings on each metal, the contaminations originating from the different metal – coating systems are gathered in Figure 55. For the aluminum plates 60 nm Al_2O_3, 45 nm HfO_2 and 44 nm Al_2O_3/HfO_2-laminate had nearly the same impact, zinc and copper concentrations being at the level of 10^9 atoms/cm^2. However, as already mentioned, with the 600 nm Al_2O_3 coating higher contamination concentrations with increased number of elements were detected when compared to the other coatings. For the titanium plates the most efficient coating was the laminate, with which no metal impurities were detected. Hafnium oxide showed the weakest passivation efficiency. For the stainless steel all impurities were brought below the detection limit with the hafnium oxide coating.

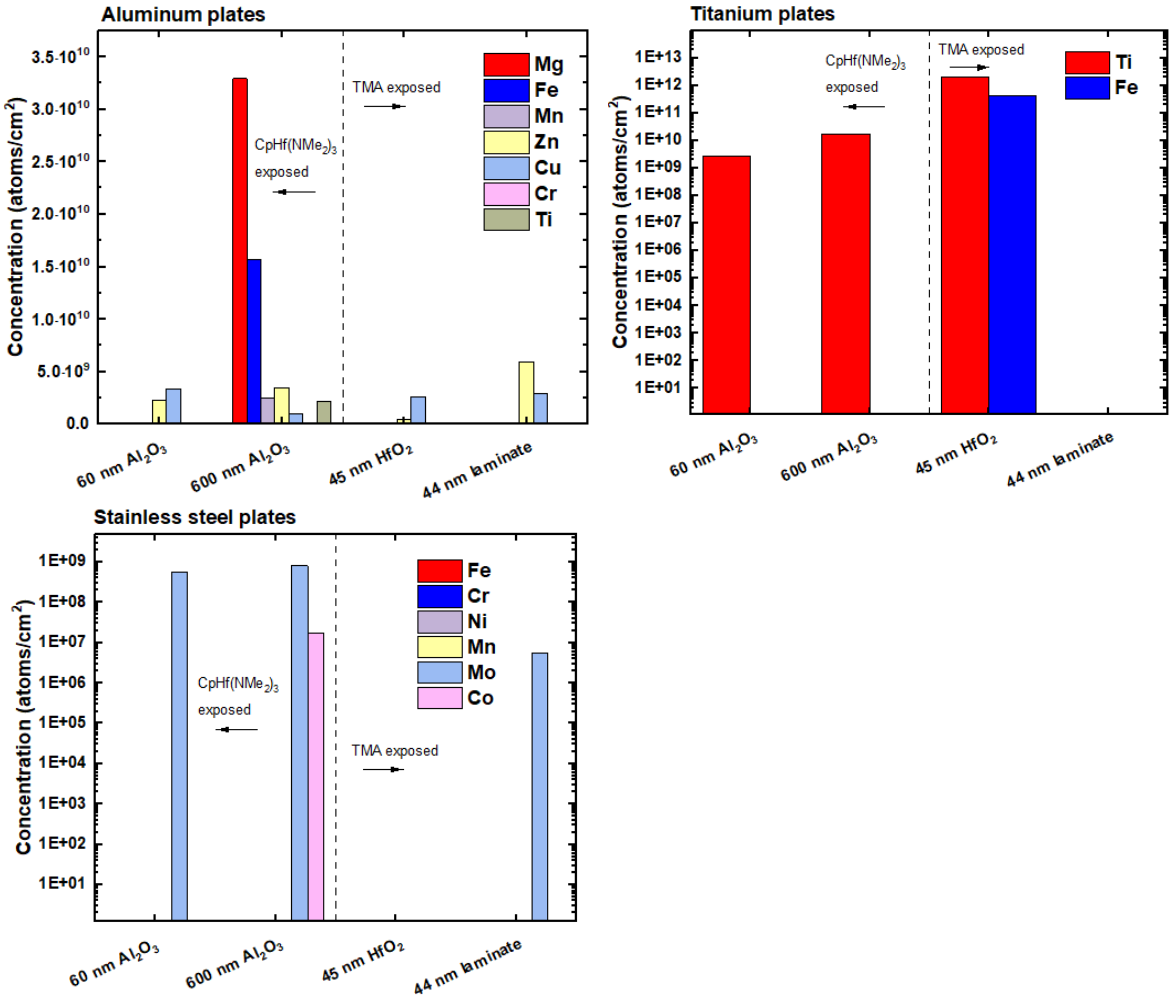

Figure 55. Metallic impurities from the aluminum, titanium and stainless steel plates with the aluminum oxide, hafnium oxide and nanolaminate coatings.

One interesting feature that can be seen from Figure 55 is that the thicker, 600 nm Al_2O_3 coating performed worse than the thinner, 60 nm Al_2O_3 coating. One factor affecting this might be cracking of the Al_2O_3 film when deposited in higher thickness.

When compared with the metal contamination specifications presented in Table 6 in the literature part of this thesis, $0.5–2 \cdot 10^{10}$ atoms/cm^2, it is noticed that with more than half of the metal – coating pairs the specification was met with all the metallic elements. This illustrates the effectivity of the ALD coatings as contamination preventing layers. However, it is important to remember that the required specification for each metal is application dependent and that the contamination studied here originated from a single metal plate, which surface area is significantly less than the whole reactor's.

12.1 Crystallinity of the HfO_2 film

To examine the crystallinity of the hafnium oxide films, XRD measurements were conducted from the HfO_2 films on silicon and titanium. The diffractograms are presented in Figure 56. Hafnium oxide on silicon was mostly amorphous based on the broad peaks in the XRD pattern. However, the structure was concluded to be partly nanocrystalline, as small peak shapes could be found from the diffractogram. On titanium, hafnium oxide was amorphous based on the detected broad peak. The other peaks originated from the titanium substrate or silicon carbide, which was used as the sand blasting agent for the metal plates. Thus, the poor diffusion barrier efficiency of HfO_2 on titanium was not comprehensively explained with its crystallinity.

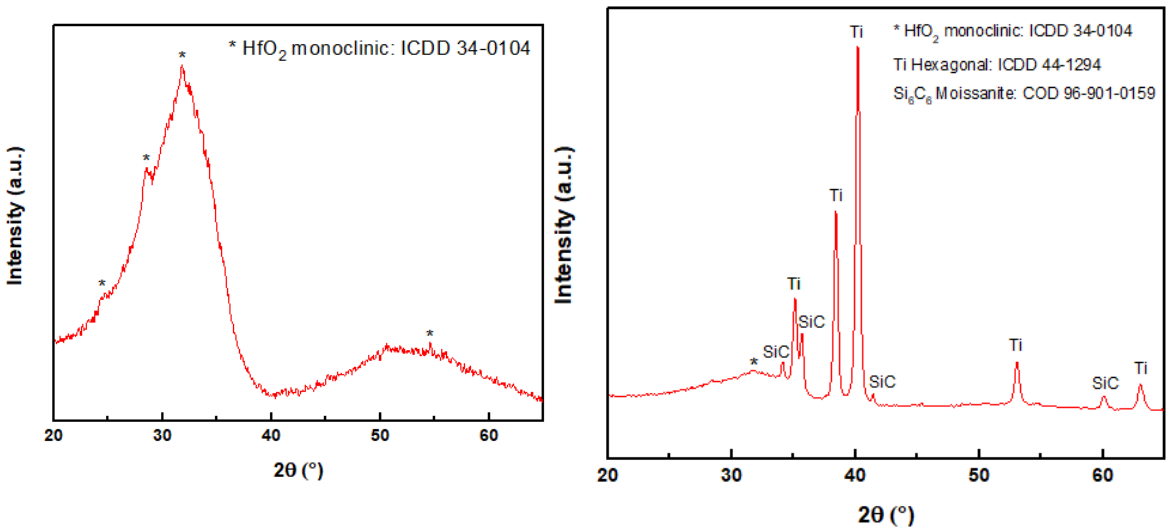

Figure 56. XRD pattern of 45 nm HfO_2 films deposited at 225 °C on silicon (left) and on titanium (right).

13. Conclusions

From the results presented above, it can be concluded that the test set-up applied worked as planned and made possible the comparison of different construction metals and the concentrations of the metallic impurities originating from them. Both research questions presented in the introduction of the experimental part were answered based on the experiments. It was shown that ALD precursors are indeed able to etch and transfer metallic species from metal surfaces or protective coatings and transfer them through gas phase on a silicon substrate. A proposed mechanism for this is presented in Figure 57. Additionally, the passivation efficiency of different protective layers, including Al_2O_3, HfO_2 and their nanolaminate was presented. It was demonstrated that metal impurity concentrations can be decreased with these coatings. It was also noticed that the underlying metal affects the passivation efficiency of the coating.

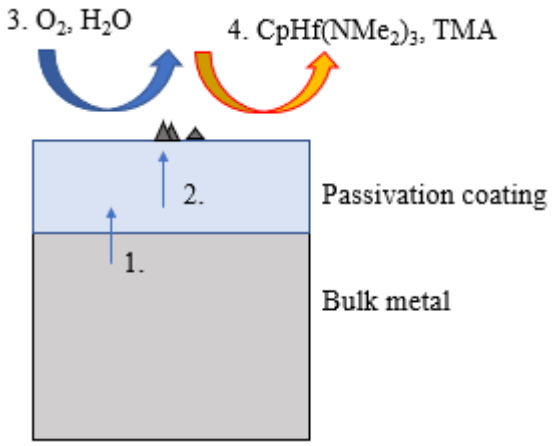

Figure 57. Transfer of metallic species 1) from the bulk metal to the passivation coating and 2) through the passivation coating to the surface followed by 3) oxidization of the metal species to oxides and 4) etching of the metal oxides by ALD precursors resulting as impurity transfer in vapour phase or through particle formation and erosion.

With the background measurements it was noticed that metal impurities were generated even when precursors were not pulsed through the chamber. These impurities can originate from the wafer itself, from handling of the wafer, or from the reactor. Regarding the analysed elements, it was noticed that gold is an especially persistent and iron a rapidly spreading element. Gold was found in high concentrations from the reactor due to previously processed samples even though the reaction chamber and cassette had been changed in between. This indicates that when sensitive products are processed, a dedicated reactor must be used. Iron originating from titanium plates was detected in higher concentrations than titanium, even though there is only 0.07 w-% of iron in the titanium plates, which demonstrates the high

diffusion capability of iron. From the precursors it was noticed that for the most metal – coating systems TMA was a more aggressive etching agent than $CpHf(NMe_2)_3$.

When the tested coatings were compared, differences were observed between various metal – coating systems. The differences between the passivation efficiencies of 60 and 600 nm Al_2O_3 coatings favored the use of the thinner coating. One possible reason for the poorer passivation efficiency of the thicker coating is its potential cracking. Additionally, especially when polished surfaces are passivated, thick layers can start cracking and peeling, which also favors the use of thinner passivation layers. 60 nm Al_2O_3, 45 nm HfO_2 and 44 nm Al_2O_3/HfO_2-laminate were all found to be effective diffusion barriers and corrosion prevention layers on at least one of the studied metals.

When choosing a protective coating for an ALD reactor, multiple factors have to be taken into account. One of these is the application of the coating to be deposited, which determines the level of metal contamination that is tolerated from the ALD processing step. Another factor is the construction material of the reactor. The selection of the reactor material can be based on the price, processability, density, chemical durability, heat expansion and conductivity of the metal. From the contamination point of view, some elements can be eliminated by choosing a construction material that does not contain them. The construction material is taken into account when the passivation coating is chosen, considering which coating provides the best passivation for the chosen metal regarding all elements or a particular element that is especially harmful for the products that will be processed in the reactor. If no remarkable differences in the passivation efficiencies between Al_2O_3 and HfO_2 are expected, aluminum oxide should be favored due to its ideal deposition chemistry, low price and amorphous nature even when deposited at relatively high temperatures. Additionally, one way to hinder metal contamination is the use of milder ALD precursors.

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